OmniVision

datasheet

PRELIMINARY SPECIFICATION

1/3.06" color CMOS 16 megapixel (4672 x 3504)
PureCel®Plus-S image sensor

OV16880 (rev 1B)

color CMOS 16 megapixel (4672 x 3504) PureCel®Plus-S image sensor

datasheet (COB)
PRELIMINARY SPECIFICATION

version 1.11
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To learn more about OmniVision Technologies, visit www.ovt.com.
OmniVision Technologies is publicly traded on NASDAQ under the symbol OVTI.

applications

- smart phones
- digital still cameras (DSC)
- digital video camcorders (DVC)
- PC multimedia

ordering information

- **OV16880-GA5A-1B-Z** (color, chip probing, 150 µm backgrinding, reconstructed wafer with good die)

features

- automatic black level calibration (ABLC)
- programmable controls for frame rate, mirror and flip, cropping, and windowing
- support for dynamic DPC cancellation
- supports output formats: 10-bit RAW RGB
- supports horizontal and vertical subsampling
- supports typical images sizes: 4672x3504, 4672x2628, 2336x1752, 1920x1080, 1280x720
- supports 2x2 binning
- standard serial SCCB interface
- up to 4-lane MIPI TX interface with speed up to 1.5 Gbps/lane
- programmable I/O drive capability
- up to 1/2/4-lane LVDS interface with speed up to 1.5 Gbps/lane
- embedded 13kbits (1664 bytes) of one-time programmable (OTP) memory for customer use
- interleave row HDR output
- support for high speed AF
- support for PDAF
- three on-chip phase lock loops (PLLs)
- programmable I/O drive capability
- built-in temperature sensor

key specifications (typical)

- **active array size:** 4672x3504
- **power supply:**
  core: 1.2V
  analog: 2.8V
  I/O: 1.8V
- **power requirements:**
  active: 300mW
  standby: 6mA
  XSHUTDN: 3µA
- **temperature range:**
  operating: -30°C to 85°C junction temperature (see **table 7-2**)
  stable image: 0°C to 60°C junction temperature (see **table 7-2**)
- **output formats:** 10-bit RGB RAW
- **lens size:** 1/3.06"
- **lens chief ray angle:** 34.2° non-linear (see **figure 9-2**)
- **maximum image transfer rate:**
  4672x3504: 30 fps (see **table 2-1**)
  4672x2628: 30 fps (see **table 2-1**)
  2336x1752: 60 fps (see **table 2-1**)
  1920x1080: 90 fps (see **table 2-1**)
  1280x720: 120 fps (see **table 2-1**)
- **input clock frequency:** 6 ~ 64 MHz
- **sensitivity:** 3200 e^-/Lux-sec
- **max S/N ratio:** 36.8 dB
- **dynamic range:** 72 dB @ 16x gain
- **scan mode:** progressive
- **pixel size:** 1.0 µm x 1.0 µm
- **dark current:** 4e^-/sec @ 60°C junction temperature
- **image area:** 4741.632 µm x 3564.288 µm
- **die dimensions:** 5640 µm x 4560 µm (COB), 5690 µm x 4610 µm (RW) (see **section 8** for details)

note COB refers to whole wafers with known good die and RW refers to singulated good die on a reconstructed wafer. Die size differs between COB and RW.

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1 signal descriptions

table 1-1 lists the signal descriptions and their corresponding pad numbers for the OV16880 image sensor. The die information is shown in **section 8**.

table 1-1 signal descriptions (sheet 1 of 3)

pad number	signal name	pad type	description
01	DOGND	ground	ground for I/O circuit
02	ADVDD	power	power for analog circuit
03	ADVDD	power	power for analog circuit
04	AGND	ground	ground for analog circuit
05	AGND	ground	ground for analog circuit
06	AVDD	power	power for analog circuit
07	AVDD	power	power for analog circuit
08	DOGND	ground	ground for I/O circuit
09	**GPIO0**	I/O	general purpose input/output 0
10	**GPIO1**	I/O	general purpose input/output 1
11	**GPIO2**	I/O	general purpose input/output 2
12	**GPIO3**	I/O	general purpose input/output 3
13	DOVDD	power	power for I/O circuit
14	AGND	ground	ground for analog circuit
15	AGND	ground	ground for analog circuit
16	PIXVDD	power	pixel analog power
17	PIXVDD	power	pixel analog power
18	AGND	ground	ground for analog circuit
19	AGND	ground	ground for analog circuit
20	AVDD	power	power for analog circuit
21	DOGND	ground	ground for I/O circuit
22	ATEST	reference	internal analog test
23	AVDD	power	power for analog circuit
24	AVDD	power	power for analog circuit
25	AGND	ground	ground for analog circuit

table 1-1 signal descriptions (sheet 2 of 3)

pad number	signal name	pad type	description
26	AGND	ground	ground for analog circuit
27	ADVDD	power	power for analog circuit
28	ADVDD	power	power for analog circuit
29	DOGND	ground	ground for I/O circuit
30	DVDD	power	power for digital circuit
31	AGND	ground	ground for analog circuit
32	AGND	ground	ground for analog circuit
33	AVDD	power	power for analog circuit
34	VH1	input	internal analog reference
35	VN2	input	internal analog reference
36	VN1	input	internal analog reference
37	DOGND	ground	ground for I/O circuit
38	DVDD	power	power for digital circuit
39	DOVDD	ground	power for I/O circuit
40	DOGND	ground	ground for I/O circuit
41	DVDD	power	power for digital circuit
42	**MDP2**	output	MIPI data positive output 2
43	**MDN2**	output	MIPI data negative output 2
44	EVDD	power	power for MIPI TX circuit
45	**MDP0**	output	MIPI data positive output 0
46	**MDN0**	output	MIPI data negative output 0
47	PVDD	power	PLL analog power
48	EGND	ground	ground for MIPI TX circuit
49	DOGND	ground	ground for I/O circuit
50	DVDD	power	power for digital circuit
51	LVDD	power	MIPI PHY driving power
52	**MCP**	output	MIPI clock positive output
53	**MCN**	output	MIPI clock negative output
54	EGND	ground	ground for MIPI TX circuit
55	**MDP1**	output	MIPI data positive output 1

table 1-1 signal descriptions (sheet 3 of 3)

pad number	signal name	pad type	description
56	MDN1	output	MIPI data negative output 1
57	EVDD	power	power for MIPI TX circuit
58	MDP3	output	MIPI data positive output 3
59	MDN3	output	MIPI data negative output 3
60	DOGND	ground	ground for I/O circuit
61	FREX	I/O	frame exposure input/mechanical shutter output
62	ILPWM	output	PWM illumination control
63	SID	input	SCCB ID select 0: SCCB device address 0x6C 1: SCCB device address 0x20
64	XVCLK	input	system clock input
65	DVDD	power	power for digital circuit
66	DOGND	ground	ground for I/O circuit
67	PWDNB	input	power down (active low with pull up resistor)
68	XSHUTDN	input	reset and power down (active low with pull down resistor)
69	DOVDD	power	power for I/O circuit
70	DVDD	power	power for digital circuit
71	DOGND	ground	ground for I/O circuit
72	SDA	I/O	SCCB interface data pin
73	SCL	input	SCCB interface input clock
74	HREF	I/O	video output horizontal signal
75	VSYNC	I/O	VSYNC output
76	STROBE	output	strobe output
77	DVDD	power	power for digital circuit
78	DOGND	ground	ground for I/O circuit
79	GPIO4	I/O	general purpose input/output 4
80	DOVDD	power	power for I/O circuit
81	DOGND	ground	ground for I/O circuit
82	DVDD	power	power for digital circuit
83	FSIN	I/O	frame sync
84	TM	input	test mode (active high with pull down resistor)

table 1-2 configuration under various conditions (sheet 1 of 2)

pad number	signal name	RESET[a]	after RESET release[b]	software standby[c]	hardware standby[d]
09	GPIO0	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
10	GPIO1	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
11	GPIO2	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
12	GPIO3	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
42	MDP2	high-z	high	high by default (configurable)	high by default (configurable)
43	MDN2	high-z	high	high by default (configurable)	high by default (configurable)
45	MDP0	high-z	high	high by default (configurable)	high by default (configurable)
46	MDN0	high-z	high	high by default (configurable)	high by default (configurable)
52	MCP	high-z	high	high by default (configurable)	high by default (configurable)
53	MCN	high-z	high	high by default (configurable)	high by default (configurable)
55	MDP1	high-z	high	high by default (configurable)	high by default (configurable)
56	MDN1	high-z	high	high by default (configurable)	high by default (configurable)
58	MDP3	high-z	high	high by default (configurable)	high by default (configurable)
59	MDN3	high-z	high	high by default (configurable)	high by default (configurable)
61	FREX	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
62	ILPWM	output zero	output zero by default (configurable)	output zero by default (configurable)	output zero by default (configurable)
63	SID	input	input	input	input
64	XVCLK	high-z	input	input	high-z
67	PWDNB	input	input	input	input
68	XSHUTDN	input	input	input	input

table 1-2 configuration under various conditions (sheet 2 of 2)

pad number	signal name	RESET[a]	after RESET release[b]	software standby[c]	hardware standby[d]
72	SDA	open drain	I/O	I/O	open drain
73	SCL	high-z	input	input	high-z
74	HREF	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
75	VSYNC	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
76	STROBE	output zero	output zero by default (configurable)	output zero by default (configurable)	output zero by default (configurable)
79	GPIO4	high-z	high-z	high-z by default (configurable)	high-z by default (configurable)
83	FSIN	high-z	input	input (configurable)	input (configurable)
84	TM	input	input	input	input

a. XSHUTDN = 0

b. XSHUTDN from 0 to 1

c. sensor set to sleep from streaming mode

d. sensor set to hardware standby from streaming mode by pulling PWDNB = 0

figure 1-1 pad diagram

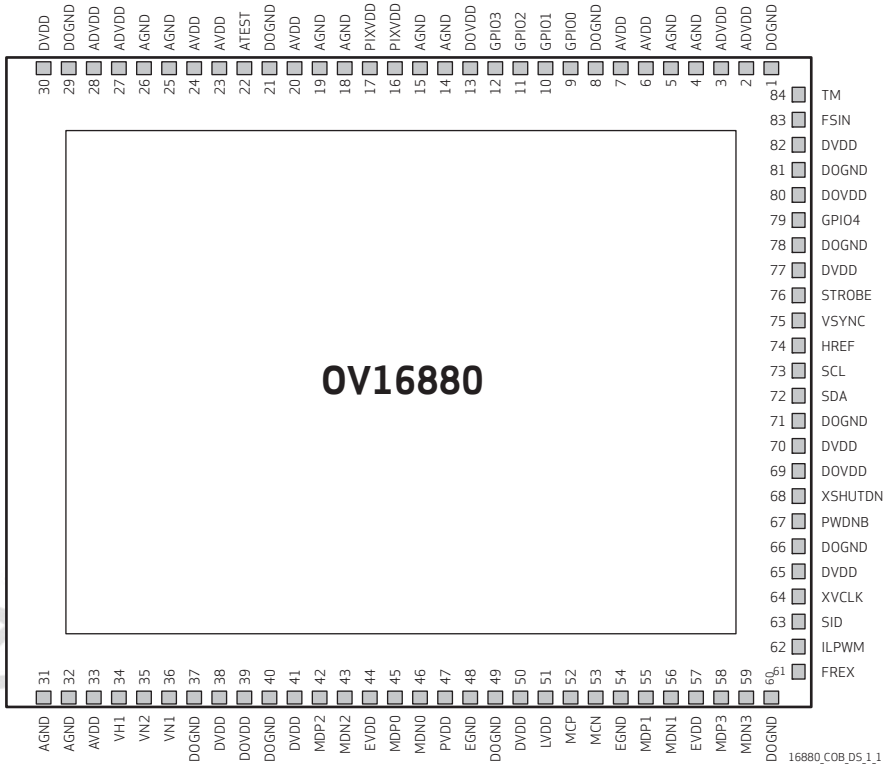


table 1-3 pad symbol and equivalent circuit (sheet 1 of 2)

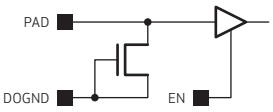
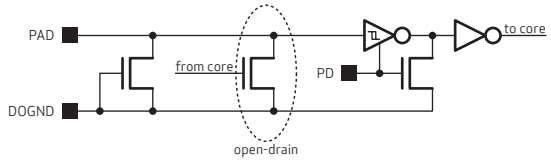
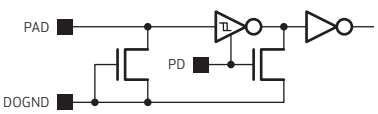
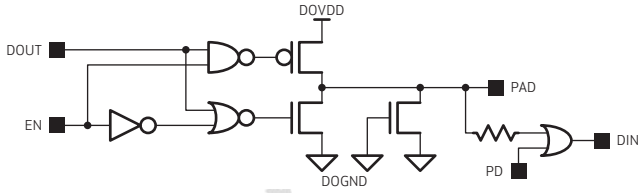
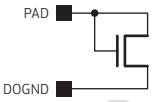
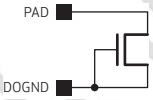
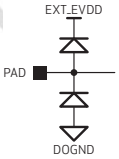
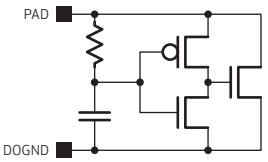
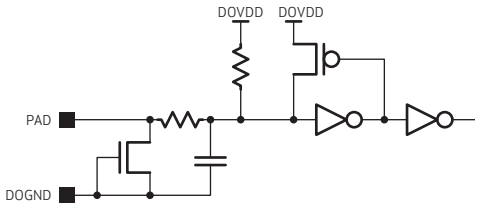
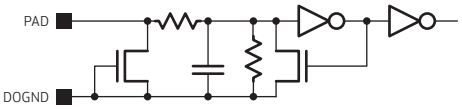
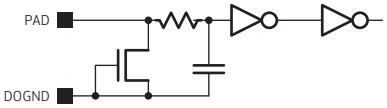
symbol	equivalent circuit
XVCLK	
SDA, GPIO4	
SCL	

table 1-3 pad symbol and equivalent circuit (sheet 2 of 2)

symbol	equivalent circuit
VSYNC, STROBE, ILPWM, FREX, FSIN, GPIO0, GPIO1, GPIO2, GPIO3, HREF	
VN1, VN2	
VH1, EGND, AGND, DOGND	
MCN, MCP, MDN0, MDP0, MDN1, MDP1, MDN2, MDP2, MDN3, MDP3	
AVDD, EVDD, DOVDD, DVDD, PVDD, PIXVDD, LVDD, PVDD, ADVDD	
PWDNB	
XSHUTDN, TM	
SID	

2 system level description

2.1 overview

The OV16880 color PureCel®Plus-S image sensor is a high performance 16 megapixel CMOS image sensor using stacked die technology that delivers (4672x3504) at 30 fps. It provides options for multiple resolutions while maintaining full field of view. Users can program image resolution, frame rate, image quality parameters. Camera functions are controlled using the industry standard serial camera control bus (SCCB).

The OV16880 is capable of delivering 30 fps at full resolution allowing burst photography at full 16 megapixel resolution. With a complete 16 megapixel image array, the OV16880 contains all the image management functions to ensure high quality imaging solutions for high resolution digital still camera (DSC), HD camcorders and mobile handsets.

All required image processing functions are programmable through the SCCB interface. In addition, OmniVision image sensors utilize proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable, color image.

2.2 architecture

The OV16880 sensor core generates streaming pixel data at a constant frame rate. **figure 2-1** shows the functional block diagram of the OV16880 image sensor.

The timing generator outputs clocks to access the rows of the imaging array, precharging and sampling rows of the array sequentially. In the time between precharging and sampling a row, the charge in the pixels decrease with exposure to incident light. This is the exposure time in rolling shutter architecture.

The exposure time is controlled by adjusting the time interval between precharging and sampling. After the data of the pixels in the row has been sampled, it is processed through analog circuitry to correct the offset and multiply the data with corresponding gain. Following analog processing is the ADC which outputs 10-bit data for each pixel in the array.

figure 2-1 OV16880 block diagram

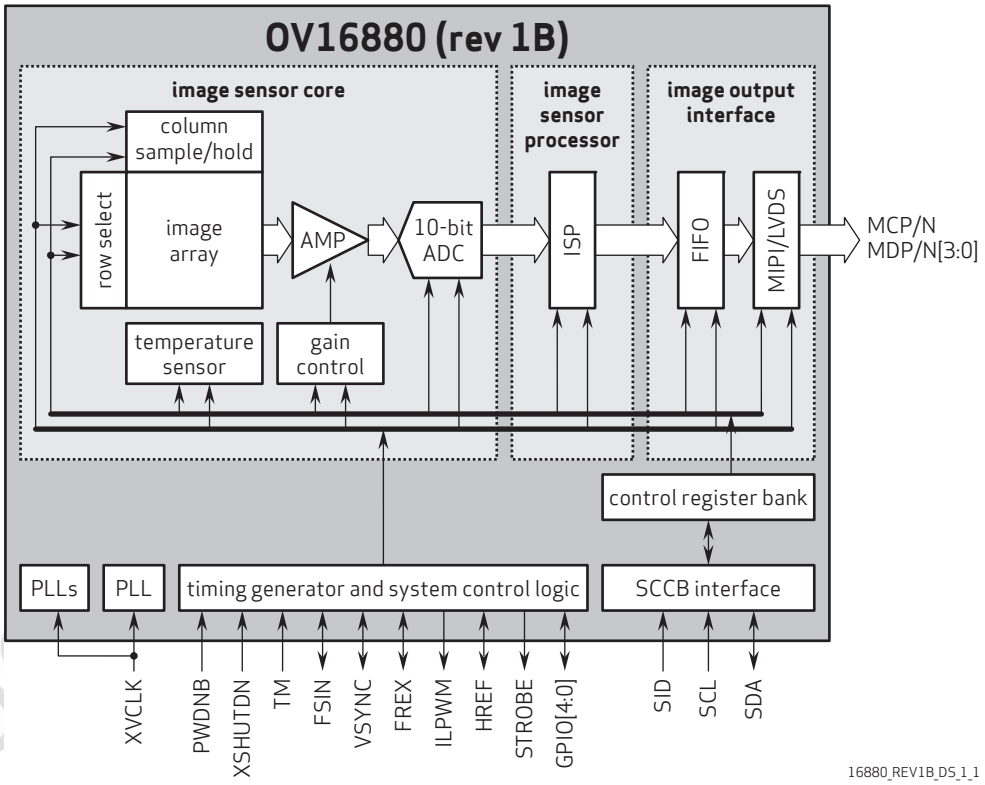
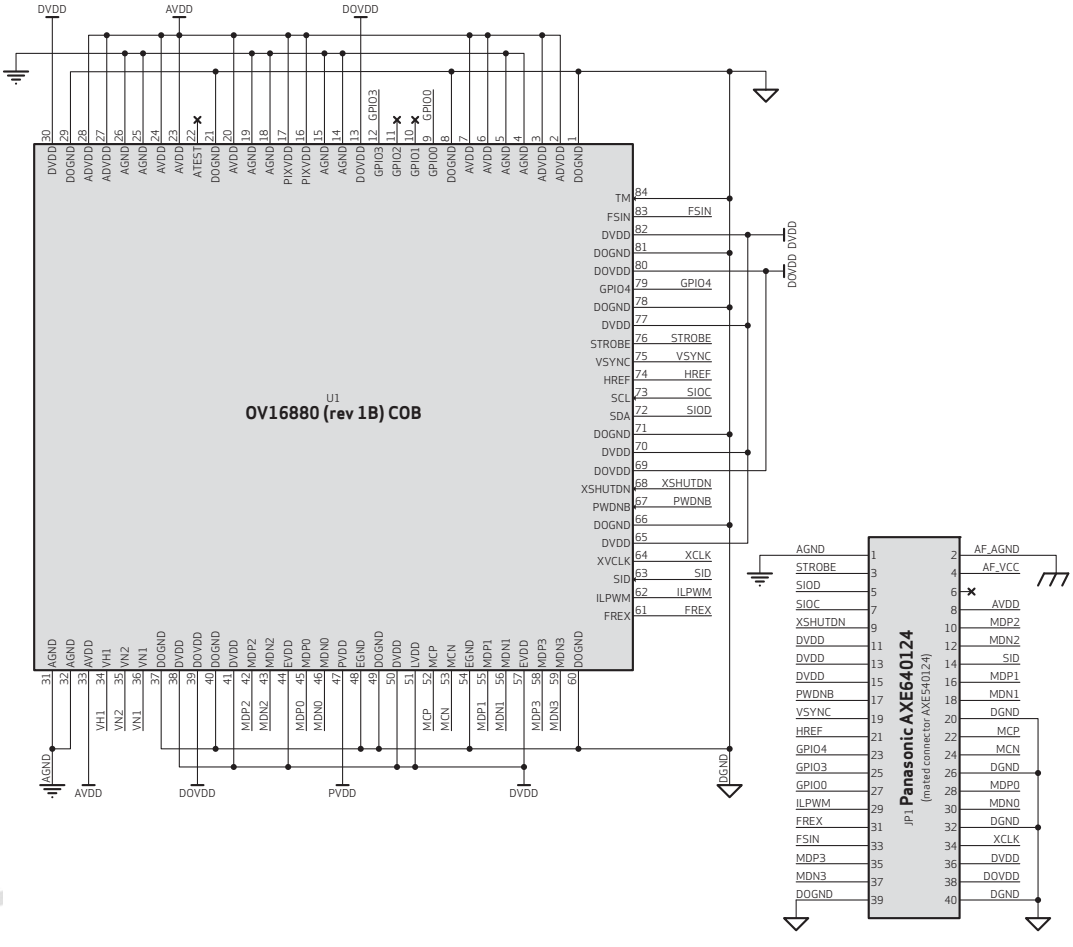


figure 2-2 OV16880 reference design schematic



note 1 PWDNB should be pulled high to DOVDD outside of module if unused.

note 2 XSHUTDOWN (XSHUTDN) should be connected to DOVDD outside of module if unused.

note 3 for other pins, such as ILPWM, FREX, FSIN, if unused, can leave floating.

note 4 AVDD is 2.8V of sensor analog power (clean).

note 5 DOVDD is 1.8/2.8V of sensor digital IO power (clean). 1.8V is recommended.

note 6 DVDD is 1.2V of sensor digital power, needs 2-3 pads on the module connector.

note 7 sensor AGND and DGND should be separated and connected to a single point outside PCB (do not connect inside the module).

note 9 capacitors should be close to their related sensor pins.

note 10 EVDD/LVDD are powers for MIPI core.
MCP and MCN are MIPI clock lane positive and negative output.
MDPx and MDNx are MIPI data lane positive and negative output.

note 11 traces of MCP, MCN, MDPx and MDNx should have the same or similar length.
differential impedance of the clock pair and data pair transmission lines should be controlled at 100 Ohm.

note 12 SID pin should be pulled low for device address 0x6C and pulled high for device address 0x20.

note 13 AF_VCC and AF_AGND is the power supply for auto focus related circuitry.
although AF_VCC is 2.8-3.3V, it is recommended to use 3.3V for better auto focus performance.

note 14 AD5823 can be used to replace AD5820.

note 15 heat release must be considered for the module.

16880_REV1B_COB_DS_2_2

2.3 format and frame

The OV16880 supports RAW RGB and HDR output with one/two/four/eight lane MIPI interface. The OV16880 also supports output formats: 10-bit normal RAW.

table 2-1 format and frame rate

format	resolution	frame rate	methodology	10-bit MIPI data rate (default)
full 16.37MP	4672x3504	30 fps	full resolution	4-lane @ 1.5 Gbps/lane
12.3MP (16:9)	4672x2628	30 fps	crop	4-lane @ 1.5 Gbps/lane
4.09MP (4:3)	2336x1752	60 fps	2x2 binning	4-lane @ 1.5 Gbps/lane
1080p	1920x1080	90 fps	2x2 binning + crop	4-lane @ 1.5 Gbps/lane
720p	1280x720	120fps	2x2 binning + crop	4-lane @ 1.5 Gbps/lane

2.4 I/O control

I/O pads on the OV16880 can be configured as inputs or outputs. The output signals can come either from a data path or registers.

table 2-2 I/O control registers (sheet 1 of 3)

function	register	description
output drive capability control	0x3009	Bit[6:5]: I/O pad drive capability 00: 1x 01: 2x 10: 3x 11: 4x
VSYNC I/O control	0x3002	Bit[7]: input/output control for VSYNC pad 0: input 1: output
VSYNC output select	0x3008	Bit[7]: output selection for VSYNC pad 0: normal data path (vertical sync signal) 1: register control value
VSYNC output value	0x3005	Bit[7]: VSYNC output value
FREX I/O control	0x3002	Bit[4]: input/output control for FREX pad 0: input 1: output
FREX output select	0x3008	Bit[5]: output selection for FREX pad 0: normal data path 1: register control value
FREX output value	0x3005	Bit[4]: FREX output value

table 2-2 I/O control registers (sheet 2 of 3)

function	register	description
STROBE output select	0x3008	Bit[4]: output selection for STROBE pad 0: normal data path 1: register control value
STROBE output value	0x3005	Bit[2]: STROBE output value
HREF I/O control	0x3002	Bit[6]: input/output control for HREF pad 0: input 1: output
HREF output select	0x3008	Bit[6]: output selection for HREF pad 0: normal data path (horizontal sync signal) 1: register control value
HREF output value	0x3005	Bit[6]: HREF output value
FSIN I/O control	0x3002	Bit[3]: input/output control for FSIN pad 0: input 1: output
FSIN output select	0x3008	Bit[3]: output selection for FSIN pad 0: normal data path (illumination control signal) 1: register control value
FSIN output value	0x3005	Bit[3]: FSIN output value
GPIO0 I/O control	0x3002	Bit[0]: input/output control for GPIO0 pad 0: input 1: output
GPIO0 output select	0x3008	Bit[0]: output selection for GPIO0 pad 0: normal data path 1: register control value (0x3663[6] should also be set to 0)
GPIO0 output value	0x3005	Bit[0]: GPIO0 output value
GPIO1 I/O control	0x3002	Bit[1]: input/output control for GPIO1 pad 0: input 1: output
GPIO1 output select	0x3008	Bit[1]: output selection for GPIO1 pad 0: normal data path 1: register control value
GPIO1 output value	0x3005	Bit[1]: GPIO1 output value
GPIO2 I/O control	0x3001	Bit[0]: input/output control for GPIO2 pad 0: input 1: output
GPIO2 output select	0x3007	Bit[0]: output selection for GPIO2 pad 0: normal data path 1: register control value

table 2-2 I/O control registers (sheet 3 of 3)

function	register	description
GPIO2 output value	0x3004	Bit[0]: GPIO2 output value
GPIO3 I/O control	0x3001	Bit[1]: input/output control for GPIO3 pad 0: input 1: output
GPIO3 output select	0x3007	Bit[1]: output selection for GPIO3 pad 0: normal data path 1: register control value
GPIO3 output value	0x3004	Bit[0]: GPIO output value
GPIO4 I/O control	0x3001	Bit[2]: input/output control for GPIO4 pad 0: input 1: output
GPIO4 output select	0x3007	Bit[2]: output selection for GPIO4 pad 0: normal data path 1: register control value
GPIO4 output value	0x3004	Bit[2]: GPIO4 output value

2.5 MIPI interface

The OV16880 supports one/two/four lanes MIPI transmitter interface at 1.5 Gbps/lane.

2.6 power management

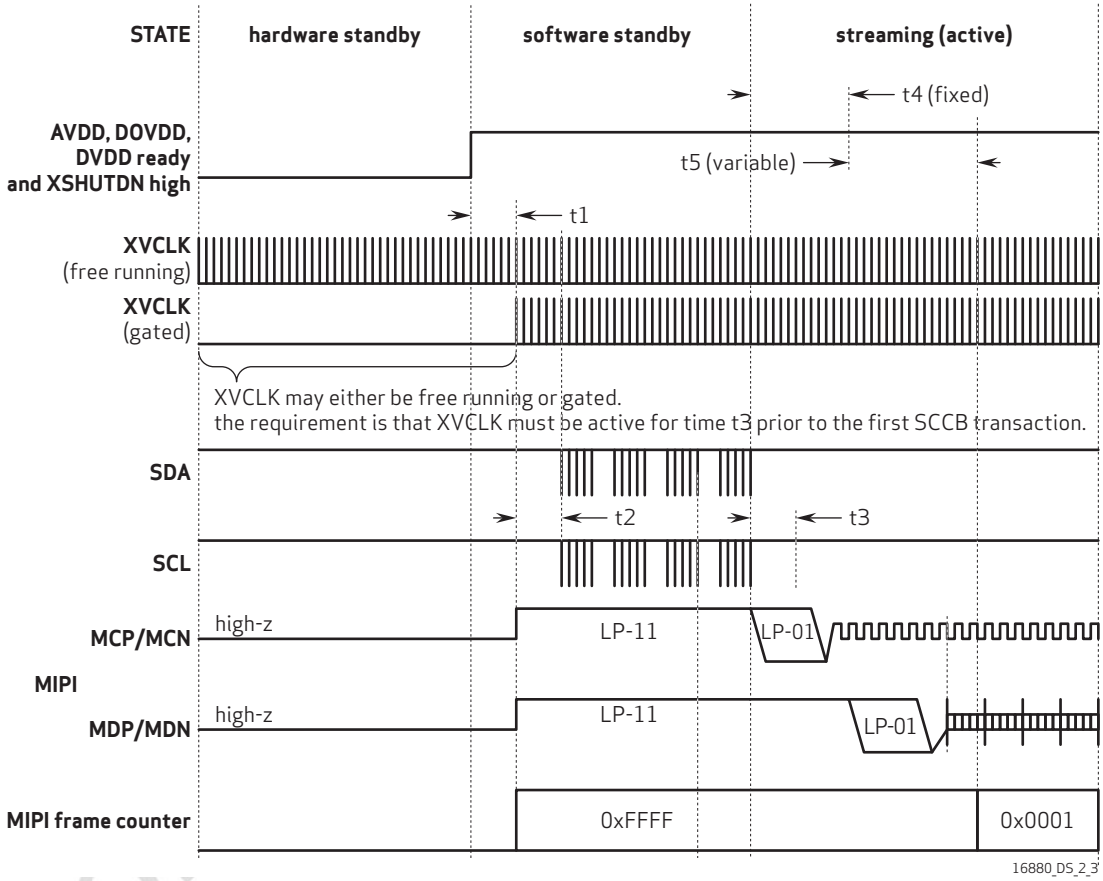
OmniVision recommends cutting off all power supplies, including the DVDD, when the sensor is not in use. There is no requirement for the power sequence. Cutting off any power source (AVDD/DVDD/DOVDD) is equivalent to XSHUTDN going low and the OV16880 will enter hardware standby mode, which uses very low power.

2.6.1 power up sequence

table 2-3 power up sequence timing constraints

constraint	label	min	max	unit
XSHUTDN rising – system ready	t1	5		ms
minimum number of XVCLK cycles prior to the first SCCB transaction	t2	8192		XVCLK cycles
PLL start up/lock time	t3		0.2	ms
entering streaming mode – first frame start sequence (fixed part)	t4		10	ms
entering streaming mode – first frame start sequence (variable part)	t5	delay is exposure time value		lines

figure 2-3 power up sequence



2.6.2 power down sequence

To avoid bad frames, OmniVision recommends using group hold to send SCCB sleep command before sending the sensor into power down mode. To set the sensor into hardware power down mode, pull XSHUTDN signal low. Any power cut is equivalent to XSHUTDN being driven low.

table 2-4 power down sequence timing constraints

constraint	label	min	max	unit
enter software standby SCCB command device in software standby mode	t0	when a frame of MIPI data is output, wait for the MIPI end code before entering the software for standby; otherwise, enter the software standby mode immediately		
minimum of XVCLK cycles after the last SCCB transaction or MIPI frame end	t1	512		XVCLK cycles
last SCCB transaction or MIPI frame end, XSHUTDN falling	t2	512		XVCLK cycles
XSHUTDN falling – AVDD falling or DOVDD falling whichever is first	t3	0.0		ns

figure 2-4 software standby sequence

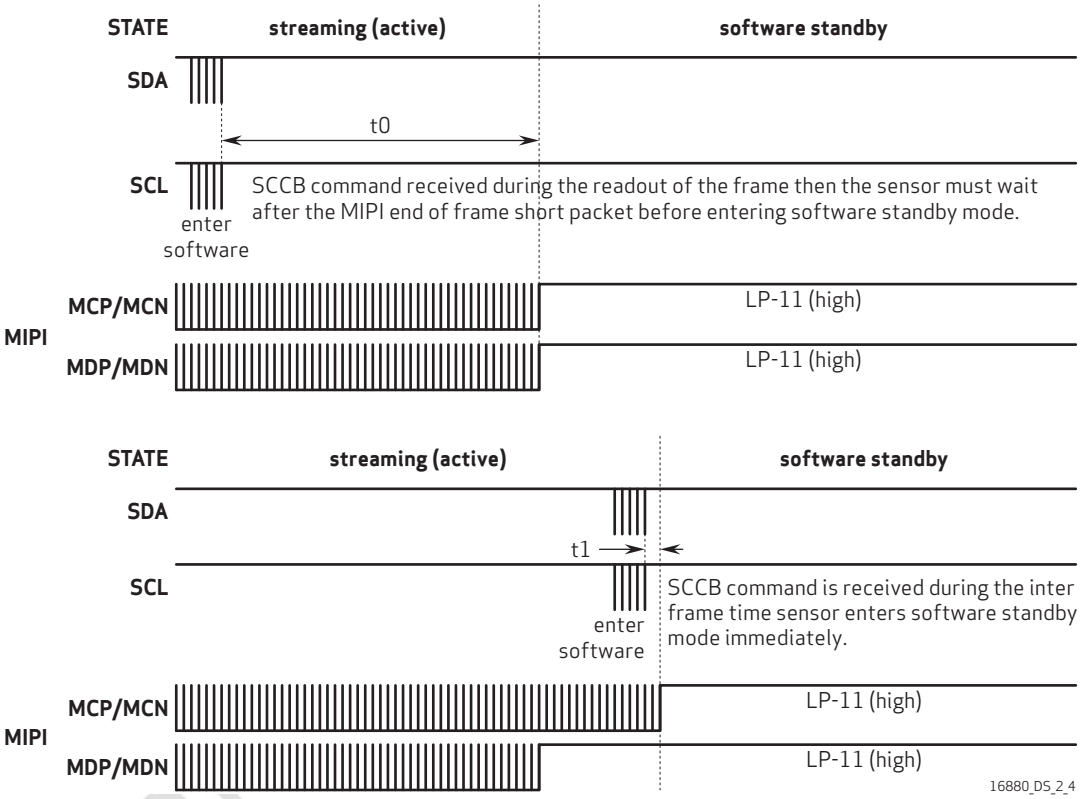
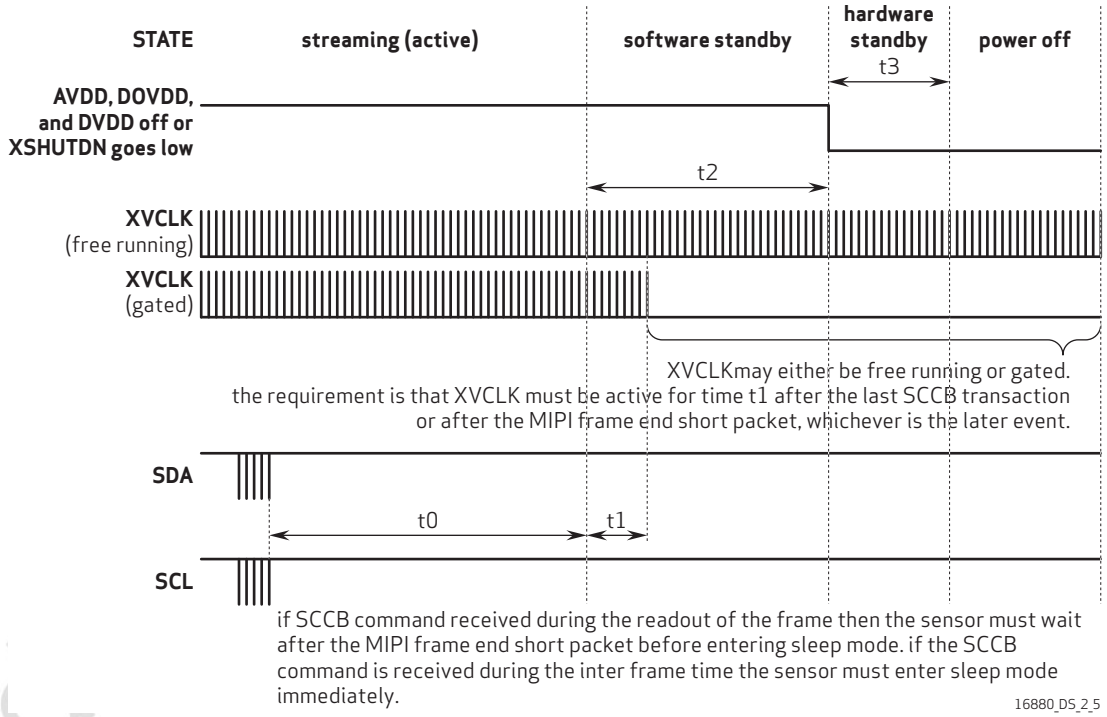


figure 2-5 power down sequence



2.7 reset

The whole chip will be reset during power up.

2.7.1 power ON reset generation

The power on reset can be controlled from the XSHUTDN pin by driving it low. Additionally, in this sensor a power on reset is generated after the internal DVDD becomes stable.

2.8 hardware and software standby

Two suspend modes are available for the OV16880:

- **hardware standby**
- **software standby**

2.8.1 hardware standby

Missing any power source (AVDD/DOVDD/DVDD) or if **XSHUTDN** is tied to low, will initiate hardware standby mode. In this mode, the total power consumption will be less than 100µW.

2.8.2 software standby

Executing a software power down (0x0100[0]) through the SCCB interface suspends internal circuit activity, but does not halt the device clock. All register content is maintained in standby mode. During the resume state, all registers are restored to their original values.

table 2-5 hardware and standby description

mode	description
hardware standby	1. enabled by pulling XSHUTDN low 2. power down all blocks 3. register values are reset to default values 4. no SCCB communication 5. minimum power consumption
software standby	1. default mode after power on reset 2. power down all blocks except SCCB 3. register values are maintained 4. SCCB communication is available 5. low power consumption 6. GPIO can be configured as high/low/tri-state

2.9 system clock control

PLL settings can only be changed during sensor standby mode (0x0100 = 0).

2.9.1 input clock

The OV16880 input clock range is 6~64 MHz.

2.9.2 PLL1

PLL1 generates a default 180 MHz pixel clock and 1.44 GHz MIPI serial clock based on 24 MHz input clock. The VCO range is from 500 MHz to 2000 MHz. A programmable clock is provided to generate different frequencies.

2.9.3 PLL2

PLL2 generates a default 288 MHz DAC clock and SRAM clock based on 24 MHz input clock. The VCO range is from 500 MHz to 1200 MHz. A programmable clock divider is provided to generate different frequencies.

2.9.4 PLL clock scheme

note
Contact your local OmniVision FAE for additional assistance on PLL configuration.

figure 2-6 clock scheme diagram

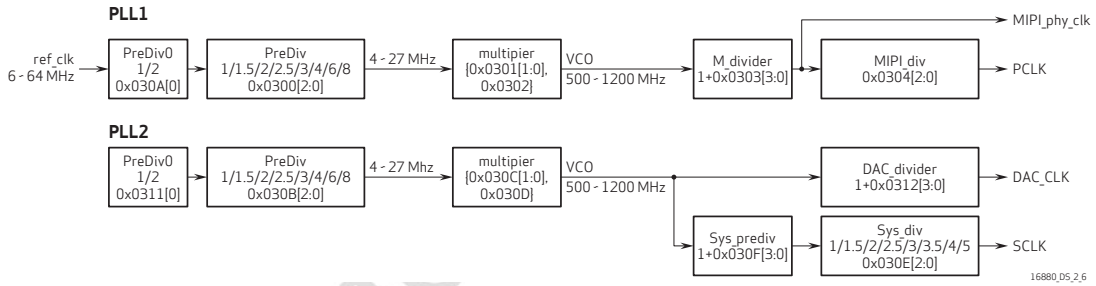


table 2-6 PLL control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x0300	PLL1 PRE DIV	0x00	RW	Bit[2:0]: PLL1 PreDiv 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x0301	PLL1 MULTI1	0x00	RW	Bit[1:0]: PLL1 multiplier[9:8]
0x0302	PLL1 MULTI0	0x3C	RW	Bit[7:0]: PLL1 multiplier[7:0]
0x0303	PLL1 DIV M	0x00	RW	Bit[3:0]: PLL1 Mdiv 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16

table 2-6 PLL control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x0304	PLL1 DIV MIPI	0x07	RW	Bit[2:0]: PLL1 MipiDiv 000: /4 001: /5 010: /6 011: /7 100: /8 Others: /8
0x0305	PLL1 DIV SP	0x01	RW	Bit[1:0]: PLL1 div_sp 00: /3 01: /4 10: /5 11: /6
0x0306	PLL1 DIV S	0x01	RW	Bit[0]: PLL1 div_s 0: /1 1: /2
0x0308	PLL1 BYP	0x00	RW	Bit[0]: PLL1 bypass
0x0309	PLL1 CP	0x01	RW	Bit[2:0]: PLL1 cp
0x030A	PLL1 CTR	0x00	RW	Bit[0]: PLL1 PreDiv0 0: /1 1: /2
0x030B	PLL2 PRE DIV	0x00	RW	Bit[2:0]: PLL2 PreDiv 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x030C	PLL2 MULTI1	0x00	RW	Bit[1:0]: PLL2 multiplier1
0x030D	PLL2 MULTI0	0x28	RW	Bit[7:0]: PLL2 multiplier0
0x030E	PLL2 DIVS	0x02	RW	Bit[2:0]: PLL2 SysDiv 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /3.5 110: /4 111: /5

table 2-6 PLL control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x030F	PLL2 DIVSP	0x03	RW	Bit[3:0]: PLL2 SysPreDiv 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16
0x0310	PLL2 CP	0x01	RW	Bit[2:0]: PLL2 cp
0x0311	PLL2 PREDIVP	0x00	RW	Bit[0]: PLL2 PreDiv0 0: /1 1: /2
0x0312	PLL CTR0	0x03	RW	Bit[4]: PLL2 bypass Bit[3:0]: PLL2 DacDiv 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16

table 2-6 PLL control registers (sheet 4 of 4)

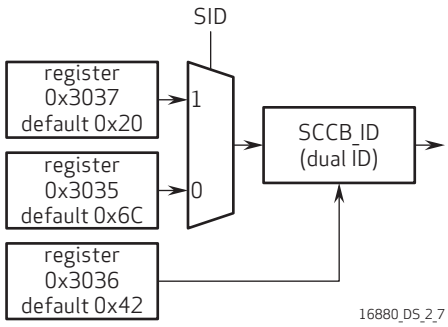
address	register name	default value	R/W	description
0x0313	PLL2 CTR1	0x00	RW	Bit[3:0]: PLL2 div SRAM 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16
0x031B	PLL1 RST	0x00	RW	Bit[0]: PLL1 rst
0x031C	PLL2 RST	0x00	RW	Bit[0]: PLL2 rst

2.10 serial camera control bus (SCCB) interface

The Serial Camera Control Bus (SCCB) interface controls the image sensor operation. Refer to the *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

In the OV16880, the sensor has two SCCB IDs. One SCCB ID is the common ID, set in register 0x3036 with a default value of 0x42. The other SCCB ID is controlled by the SID pin. If the SID pin is low, the SCCB ID comes from register 0x3035, which has a default value of 0x6C. If the SID pin is high, the SCCB ID comes from register 0x3036. Registers 0x3035, 0x3036, and 0x3037 values can be changed after power up through SCCB control.

figure 2-7 SCCB ID structure



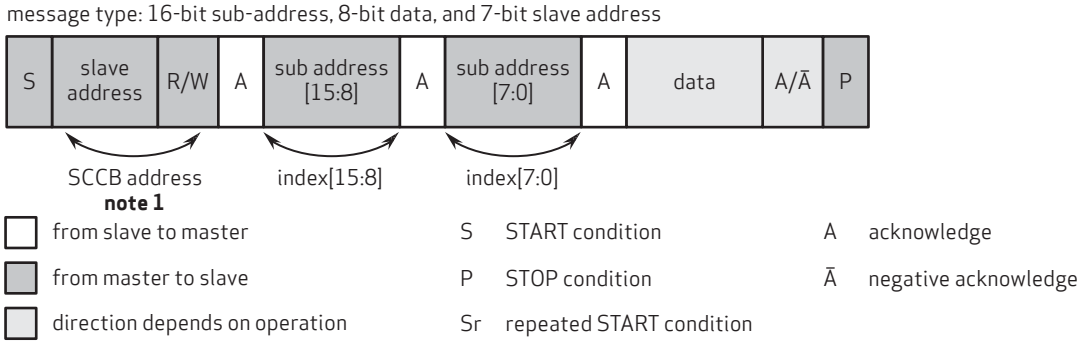
2.10.1 data transfer protocol

Data transfer of the OV16880 follows the SCCB protocol.

2.10.2 message format

The OV16880 supports the message format shown in **figure 2-8**. The repeated START (Sr) condition is not shown in **figure 2-8**, but is shown in **figure 2-9** and **figure 2-11**.

figure 2-8 message type



note 1 slave address must be 0x36 for SCCB write address to be 0x6C and for SCCB read address to be 0x6D

16880_DS_2_8

2.10.3 read / write operation

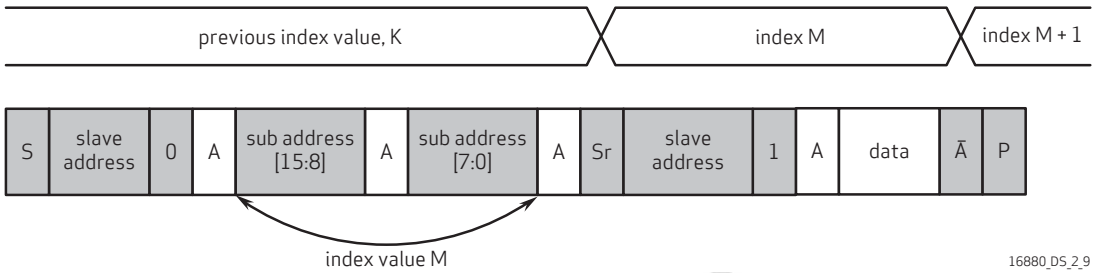
The OV16880 supports four different read operations and two different write operations:

- a single read from random locations
- a sequential read from random locations
- a single read from current location
- a sequential read from current location
- single write to random locations
- sequential write starting from random location

The sub-address in the sensor automatically increases by one after each read/write operation.

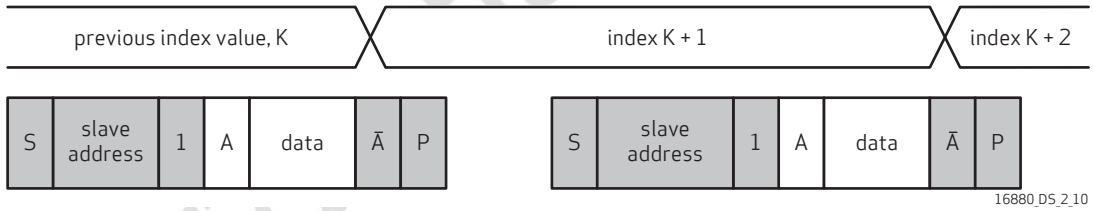
In a single read from random locations, the master does a dummy write operation to desired sub-address, issues a repeated start condition and then addresses the camera again with a read operation. After acknowledging its slave address, the camera starts to output data onto the SDA line as shown in **figure 2-9**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-9 SCCB single read from random location



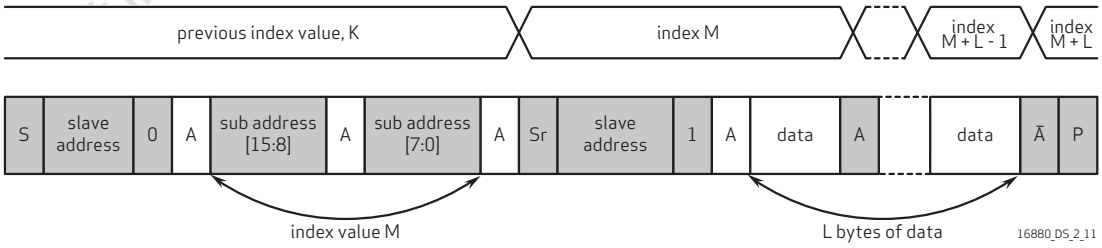
If the host addresses the camera with read operation directly without the dummy write operation, the camera responds by setting the data from last used sub-address to the SDA line as shown in **figure 2-10**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-10 SCCB single read from current location



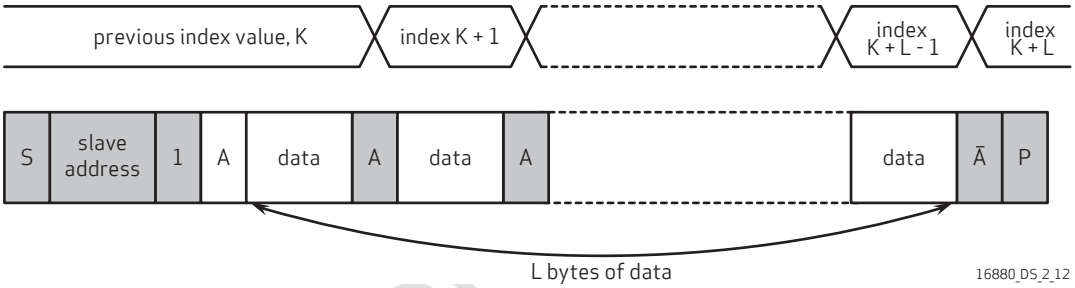
The sequential read from a random location is illustrated in **figure 2-11**. The master does a dummy write to the desired sub-address, issues a repeated start condition after acknowledge from slave and addresses the slave again with read operation. If a master issues an acknowledge after receiving data, it acts as a signal to the slave that the read operation shall continue from the next sub-address. When master has read the last data byte, it issues a negative acknowledge and stop condition.

figure 2-11 SCCB sequential read from random location



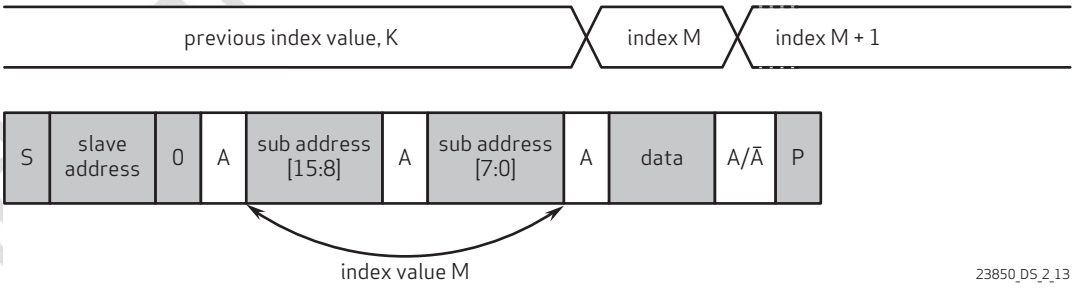
The sequential read from current location is similar to a sequential read from a random location. The only exception is that there is no dummy write operation. as shown in **figure 2-12**. The master terminates the read operation by setting a negative acknowledge and stop condition.

figure 2-12 SCCB sequential read from current location



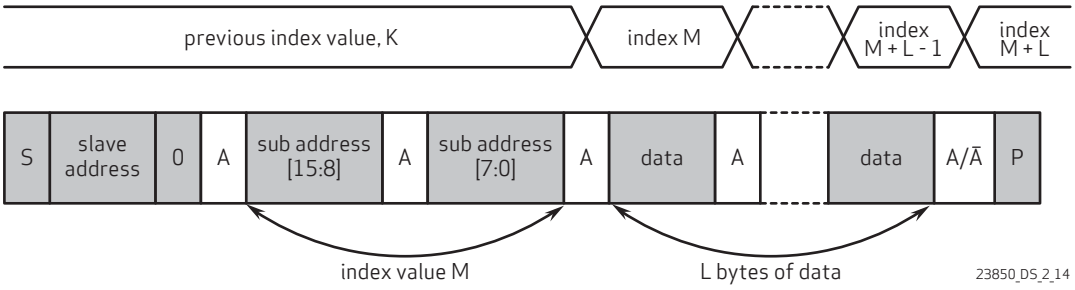
The write operation to a random location is illustrated in **figure 2-13**. The master issues a write operation to the slave, sets the sub-address and data correspondingly after the slave has acknowledged. The write operation is terminated with a stop condition from the master.

figure 2-13 SCCB single write to random location



The sequential write is illustrated in **figure 2-14**. The slave automatically increments the sub-address after each data byte. The sequential write operation is terminated with stop condition from the master.

figure 2-14 SCCB sequential write to random location



2.10.4 SCCB timing

figure 2-15 SCCB interface timing

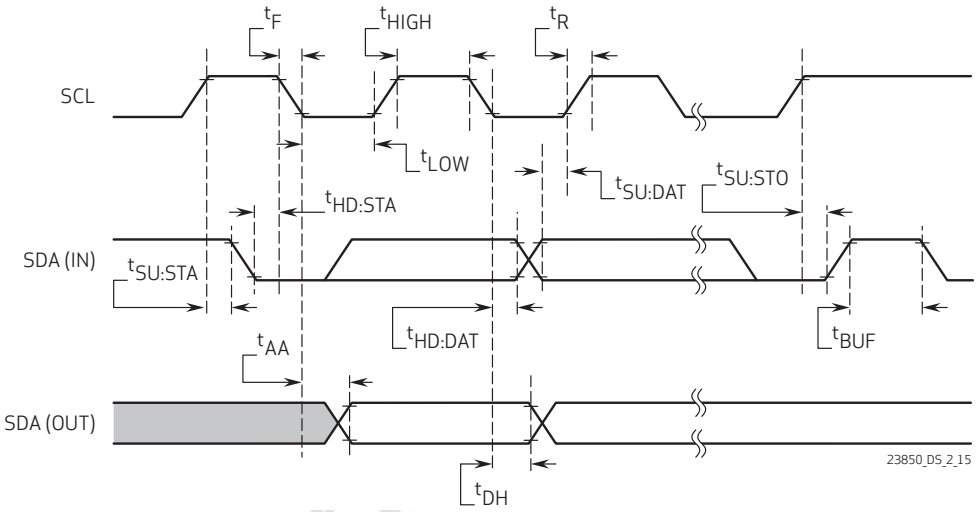


table 2-7 SCCB interface timing specifications[ab]

symbol	parameter	min	typ	max	unit
f_{SCL}	clock frequency			400	kHz
t_{LOW}	clock low period	1.3			µs
t_{HIGH}	clock high period	0.6			µs
t_{AA}	SCL low to data out valid	0.1		0.9	µs
t_{BUF}	bus free time before new start	1.3			µs
$t_{HD:STA}$	start condition hold time	0.6			µs
$t_{SU:STA}$	start condition setup time	0.6			µs
$t_{HD:DAT}$	data in hold time	0			µs
$t_{SU:DAT}$	data in setup time	0.1			µs
$t_{SU:STO}$	stop condition setup time	0.6			µs
t_R, t_F	SCCB rise/fall times			0.3	µs
t_{DH}	data out hold time	0.05			µs

a. SCCB timing is based on 400kHz modes

b. timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 30%, timing measurement shown in the medium of the rising/falling edge signifies 50%, timing measurement shown at the beginning of the rising edge and/or of the falling edge signifies 70%

2.11 group write

Group write is supported in order to update a group of registers (except 0xFFFx) in the same frame. These registers are guaranteed to be written prior to the internal latch at the frame boundary.

The OV16880 supports up to four groups can be recorded in the same frame. These groups share 1024 bytes of memory and the size of each group is programmable by adjusting the start address.

table 2-8 context switching control

address	register name	default value	R/W	description
0x3208	GROUP ACCESS	–	W	Group Access Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group delay launch 1110: Group quick launch Others: Debug mode Bit[3:0]: Group ID 0000: Group bank 0, default start from address 0x00 0001: Group bank 1, default start from address 0x40 0010: Group bank 2, default start from address 0x80 0011: Group bank 3, default start from address 0xB0 Others: Debug mode
0x3209	GROUP0 PERIOD	0x00	RW	Bit[6:5]: Switch back group In context switch, it must be group 0 Bit[4:0]: Number of frames to stay in first group
0x320A	GROUP1 PERIOD	0x00	RW	Number of Frames to Stay in Second Group
0x320B	GRP_SWCTRL	0x01	RW	Bit[7]: Auto switch Bit[3]: group_switch_repeat_en Enable the first group (group 0) and second group repeatable switch Bit[2]: context_en Enable to switch from second group back to first group (group 0) automatically Bit[1:0]: Second group selection
0x320D	GRP_ACT	–	R	Active Group Indicator
0x320E	FM_CNT_GRP0	–	R	Group 0 Frame Count
0x320F	FM_CNT_GRP1	–	R	Group 1 Frame Count

2.12 hold

After the groups are configured, users can perform a hold operation to store register settings into the SRAM of each group. The hold of each group starts and ends with control register 0x3208. The lower 4 bits of register 0x3208 control which group to access, and the upper 4 bits control the start (0x0: hold start) and end (0x1: hold end) of the hold operation.

The example setting below shows the sequence to hold group 0:

```
6C  3208  00    group 0 hold start
6C  3800  11    first register into group 0
6C  3911  22    second register into group 0
6C  3208  10    group 0 hold end
```

2.13 launch

After the contents of each group are defined in the hold operation, all registers belonging to each group are stored in SRAM and ready to be written into target registers (i.e., the launch of that group).

There are five launch modes as described in **section 2.13.1** to **section 2.13.5**.

2.13.1 launch mode 1 - quick manual launch

Manual launch is enabled by setting register 0x320B to 0.

Quick manual launch is achieved by writing to control register 0x3208. The value written into this register is 0xEX, the upper 4 bits (0xE) are the quick launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 0, they just write the value 0xE0 to register 0x3208, then the contents of group 0 will be written to the target registers immediately after the sensor gets this command through the SCCB. Below is an example of this setting.

```
6C  320B  00    manual launch on
6C  3208  E0    quick launch group 0
```

2.13.2 launch mode 2 - delay manual launch

Delay manual launch is achieved by writing to register 0x3208. The value written into this register is 0xAX, where the upper 4 bits (0xA) are the delay launch command and the lower 4 bits (0xX) are the group number. For example, if users want to launch group 1, they just write the value 0xA1 to register 0x3208, then the contents of group 1 will be written to the target registers. The difference with mode 1 is that the writing will wait for some internally defined time spot in vertical blanking; thus delayed. Below is an example of this setting.

```
6C  320B  00    manual launch on
6C  3208  A1    delay launch group 1
```

2.13.3 launch mode 3 - quick auto launch

Quick auto launch works like the mode 1, but the difference is it will return to a specified group automatically. This is controlled by the register 0x3209, where bit[6:5] controls which group to return and bit[4:0] controls how many frames to stay before returning. The auto launch enable bit is the 0x320B[7]. The operation can be better understood with an example of this setting:

```
6C  3209  44    Bit[6:5]: 2, return to group 2, Bit[4:0]: 4: stay 4 frames
6C  320B  80    auto launch on
6C  3208  E0    quick launch group 0
```

In this example, the sensor will quick launch group 0, stay at group 0 for 4 frames, and then return to group 2.

2.13.4 launch mode 4: delay auto launch

Delay auto launch works like mode 2 in the delay launch part and like the mode 3 in the return part.

The operation can be better understood with an example of this setting:

```
6C  3209  44    Bit[6:5]: 2, return to group 2, Bit[4:0]: 4: stay 4 frames
6C  320B  80    auto launch on
6C  3208  A0    delay launch group 0
```

In this example, the sensor will delay launch group 0, stay at group 0 for 4 frames, and then return to group 2.

2.13.5 launch mode 5: repeat launch

Repeat launch is controlled by registers 0x3209, 0x320A, and 0x320B. In this mode, the launch is repeated automatically between the first group (must be group 0) and the second group (can be either one of groups 1-3, which is specified by register 0x320B[1:0]). Register 0x3209 defines how many frames remain in group 0 and register 0x320A defines how many frames remain in the second group.

The operation can be better understood with an example of this setting:

```
6C  3209  02    Bit[4:0]: 2, stay 2 frames in group 0
6C  320A  03    Bit[7]: 3, stay 3 frames in the second group
6C  320B  0E    Bit[3:2]: 3, repeat launch on, Bit[1:0]: 2, second group select:
                group 2
6C  3208  A0    always use a0 for repeat launch
```

In this example, the sensor will delay launch group 0, stay at group 0 for 2 frames, then switch to group 2 for 3 frames, then back to group 0 for 2 frames, group 2 for 3 frames and so on.

Below is another example that shows applying launch mode 2 (delay manual launch) first, the sensor stays at group 2 for an indefinite number of frames, and then applying launch mode 5 (repeat launch). The sensor will switch to group 0 for 2 frames, then group 2 for 3 frames, and so on.

```
6C  320B  00    manual launch on
6C  3208  A2    delay launch group 2 stay at group 2 for indefinite frames
6C  3209  02    Bit[4:0]: 2, stay 2 frames in group 0
6C  320A  03    Bit[7:0]: 3, stay 3 frames in the second group
6C  320B  0E    Bit[3:2]: 3, repeat launch on, Bit[1:0]: 2, second group select:
                group 2
6C  3208  A0    always use A0 for repeat launch
```

Switch to group 0 for 2 frames, then group 2 for 3 frames, and so on.

3 block level description

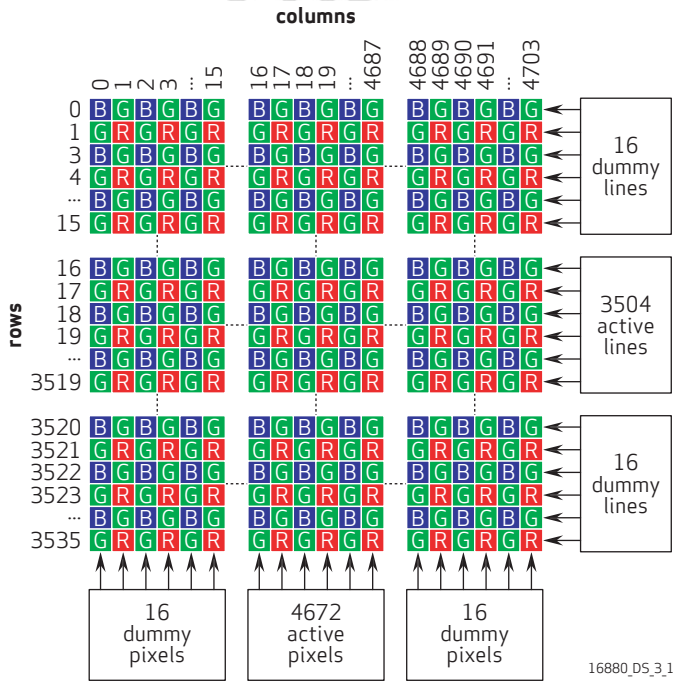
3.1 pixel array structure

The OV16880 sensor has an image array of 4704 columns by 3536 rows (16,733,440 pixels). **figure 3-1** shows a cross-section of the image sensor array.

The color filters are arranged in a Bayer pattern. The primary color BG/GR array is arranged in line-alternating fashion. Of the 16,633,344 pixels, 16,370,688 (4672x3504) are active pixels and can be output. The other pixels are used for black level calibration and interpolation.

The sensor array design is based on a field integration readout system with line-by-line transfer and an electronic shutter with a synchronous pixel readout scheme.

figure 3-1 sensor array region color filter layout



3.2 HDR mode

The OV16880 sensor supports two HDR modes. The HDR control bits are 0x3821[7:6].

```
0x3821[7:6]:
00: non-HDR mode
01: 2-exposure HDR mode
```

In 2-exposure HDR, the exposure is still controlled by a rolling shutter. However, the frame data is separated into "exposure 1" and "exposure 2" in every two rows, shown in **figure 3-2**.

Exposure 1 time is controlled by registers 0x3501 and 0x3502. Gain 1 is controlled by registers0x350A and 0x350B.

Exposure 2 time is controlled by registers 0x3507, and 0x3508. Gain2 is controlled by registers 0x354E and 0x354F.

figure 3-2 2-exposure diagram

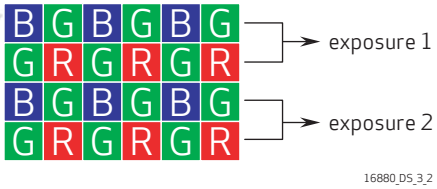


table 3-1 HDR control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3501	MEC LONG EXPO	0x00	RW	Long Exposure Bit[7:0]: Long exposure[15:8]
0x3502	MEC LONG EXPO	0x02	RW	Long Exposure Bit[7:0]: Long exposure[7:0]
0x3507	MEC MEDIUM EXPO	0x00	RW	Medium Exposure Bit[6:0]: Medium exposure[14:8]
0x3508	MEC MEDIUM EXPO	0x02	RW	Medium Exposure Bit[7:0]: Medium exposure[7:0]
0x350A	MEC LONG GAIN	0x00	RW	Long Gain Bit[2:0]: Long gain[10:8]
0x350B	MEC LONG GAIN	0x10	RW	Long Gain Bit[7:0]: Long gain[7:0]
0x354E	MEC MEDIUM GAIN	0x00	RW	Medium Gain Bit[2:0]: Medium gain[10:8]
0x354F	MEC MEDIUM GAIN	0x10	RW	Medium Gain Bit[7:0]: Medium gain[7:0]

table 3-1 HDR control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3821	TIMING_FORMAT2	0x18	RW	Bit[7:6]: hdr_en[1:0] Works only when 0x5005[0] = 0 00: Non-HDR 01: HDR2 1x: Not used

3.3 binning

Binning mode is usually used for low resolution. When the binning function is ON, voltage levels of adjacent pixels are averaged. If the binning function is OFF, the pixels, which are not output, are merely skipped. The OV16880 supports 2x2 binning and 4x4 binning. **figure 3-3** illustrates vertical fast binning, where the voltage levels of two vertical adjacent same-color pixels are averaged before entering the ADC. Horizontal binning is applied by the ISP DCW block.

figure 3-3 example of 2x2 binning

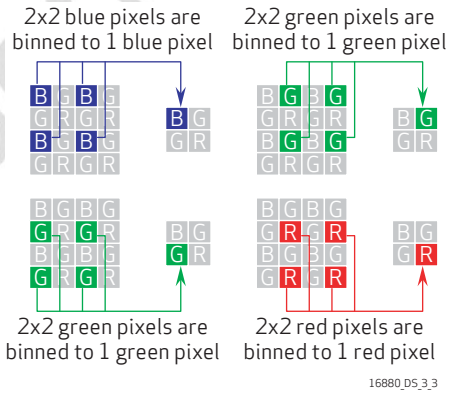


figure 3-4 example of 4x4 binning

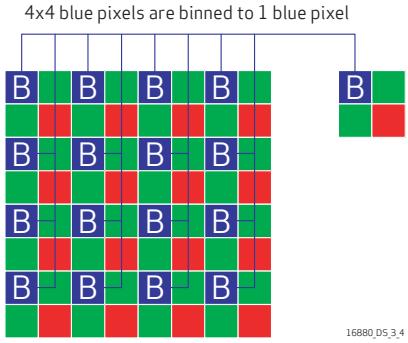


table 3-2 binning-related registers

address	register name	default value	R/W	description
0x3820	TIMING_FORMAT1	0x00	RW	Bit[1:0]: Vertical binning 01: Vertical binning 2
0x3842	TIMING_FORMAT2	0x00	RW	Bit[6]: Horizontal binning 2
0x5000	ISP_DCW	0x8E	RW	Bit[6]: Horizontal DCW enable Bit[6]: Vertical DCW enable

3.4 analog amplifier

When the column sample/hold circuit has sampled one row of pixels, the pixel data will shift out one-by-one into an analog amplifier.

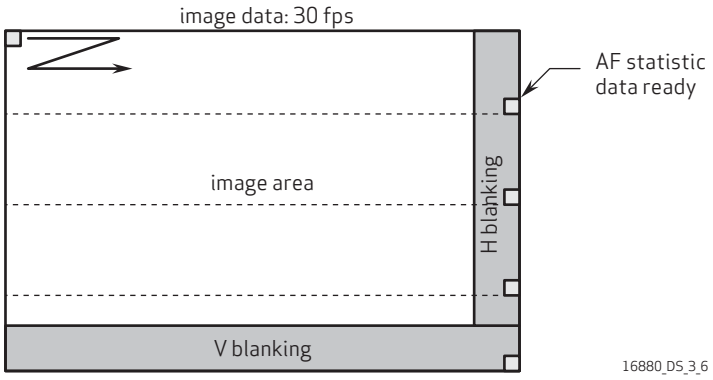
3.5 12-bit A/D converters

The balanced signal is then digitized by the on-chip 12-bit ADC.

3.6 fast auto focus (AF) control

The OV16880 has programmable AF lines for high speed auto focus. The positions of those AF lines can be programmed by registers. The AF lines frame rate is also programmable (1x, 2x, 3x, or 4x of normal image frame rate). Because AF lines run at a higher frame rate of up to 4x of normal image data, the backend chip can receive focus information faster than traditional auto focus. With a high speed actuator, the auto focus is faster. There are two types of AF data: AF lines raw data and statistics data. The AF data can be output via SCCB (registers), through MIPI data type or virtual channel. Below is an example of AF statistic data output. For details of fast AF, please contact your local OmniVision FAE.

figure 3-5 AF statistics data



3.7 PDAF control

The OV16880 supports PDAF data output through MIPI by programmable data type mode or virtual channel mode. All PDAF data or partial of them are selected to be output. The OV16880 is a type 3 PD sensor, which means the sensor can output a PD pixel corrected image along with PD data.

3.7.1 PDAF data output: option 1 (SCCB interface, sensor is slave)

The backend chip can read the sensor's register through MCU to get the PDAF data. PDAF data are stored in a 8k memory with start address 0xD000.

3.7.2 PDAF data output: option 2 (programmable data type)

Option 2 uses programmable data type for PDAF raw data. Set register 0x3661[1:0] to 1 to enable PDAF output timing and set register 0x486E[3] to 1 to enable MIPI data type mode. Register 0x4809[5:0] is the data type of the PD data. PDAF data is output during image data horizontal blanking. The maximum PDAF data number in one package is configured by registers {0x4640, 0x4641}×8.

3.7.3 PDAF data output: option 3 (MIPI virtual channel)

Option 3 is the MIPI virtual channel for PDAF raw data. Set register 0x3661[1:0] to 3 to enable PDAF output timing and set register 0x486E[2] to 1 to enable MIPI virtual channel mode. A normal image outputs through MIPI virtual channel 0. The PDAF data outputs through MIPI virtual channel 1. PDAF data is output during image data horizontal blanking. The maximum PDAF data number in one package is configured by registers {0x4640, 0x4641}×8.

figure 3-6 PDAF data output diagram

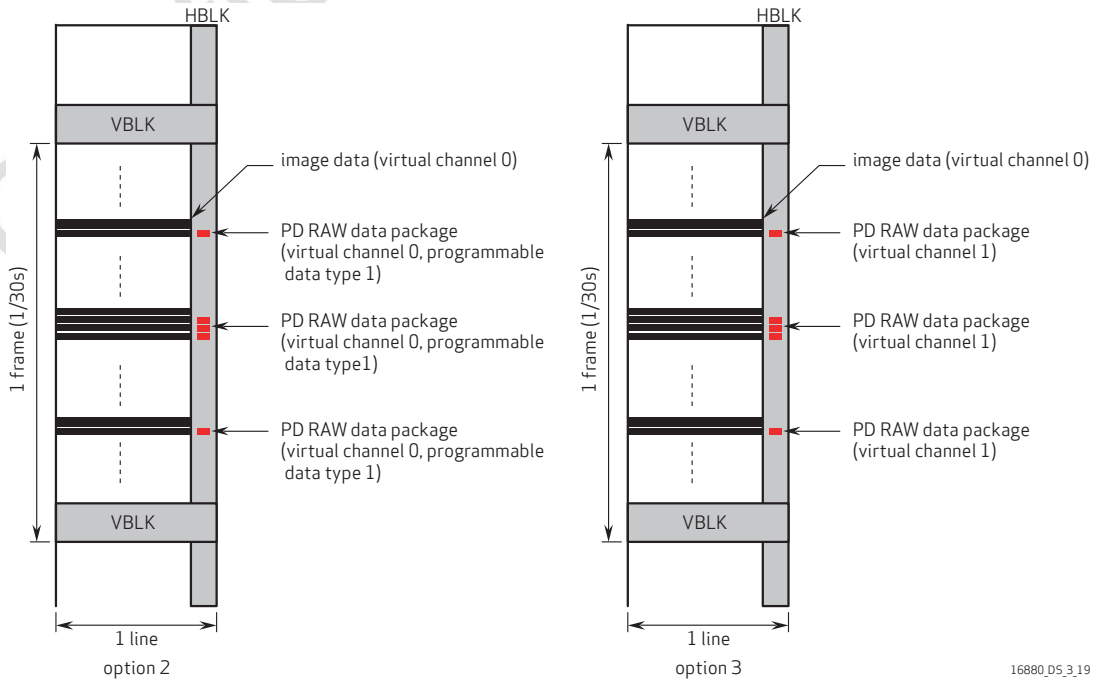


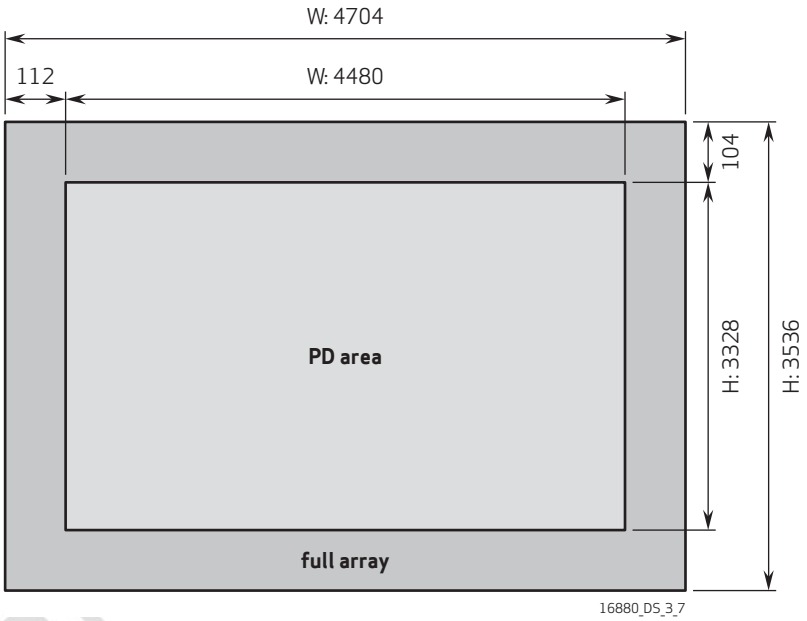
table 3-3 PDAF control registers

address	register name	default value	R/W	description
0x3661	PDAF CONTROL	0x04	RW	Bit[1]: PDAF control 0: PD data type mode enable 1: PD virtual channel mode enable Bit[0]: MIPI timing align enable
0x366C	2X4 LANE MIPI CONTROL	0x00	RW	Bit[7:3]: Not used Bit[2]: Half line mode timing align option 0: First half row first, second half row next mode 1: Same time mode Bit[1:0]: MIPI 2x4 line mode 00: Function disable 01: Even-odd pixel mode 10: 4 pixel mode 11: Half row mode
0x4640	PD FIFO CONTROL	0x01	RW	Bit[7:0]: PD data max number high byte/8 in one package
0x4641	PD FIFO CONTROL	0x04	RW	Bit[7:0]: PD data max number low byte/8 in one package
0x4809	MIPI CONTROL	0x2B	RW	Bit[5:0]: PDAF data type
0x486E	MIPI CONTROL	0x03	RW	Bit[3]: Data type mode enable Bit[2]: Virtual channel mode enable

3.8 PD pixel arrangement

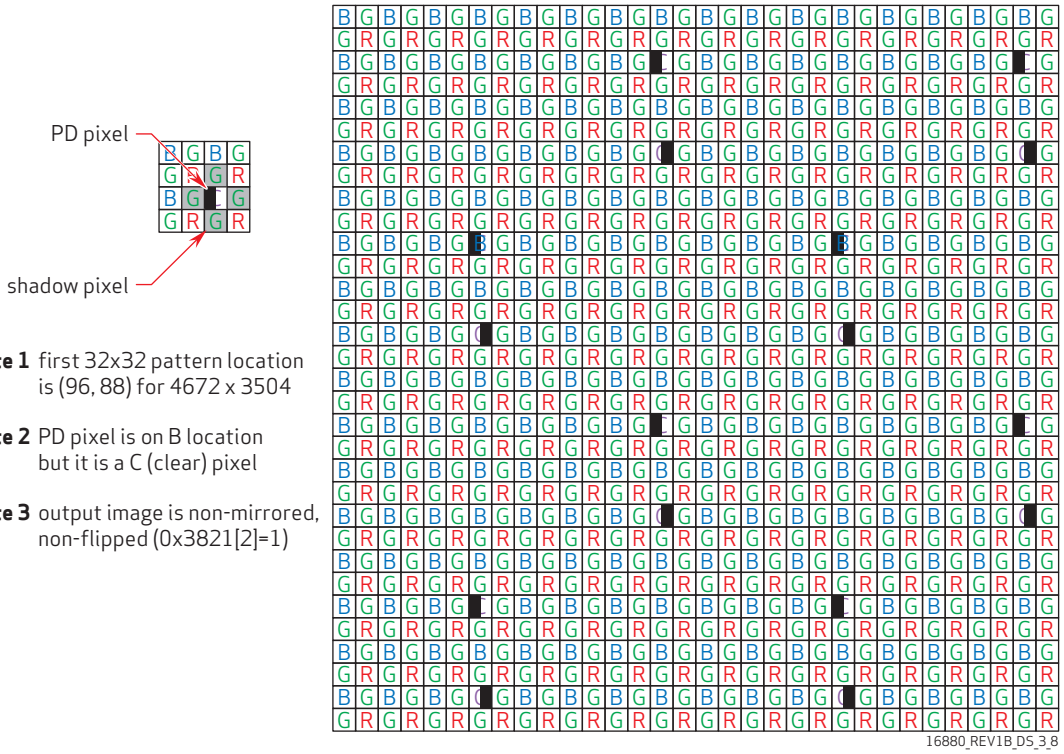
PD pixels are evenly arranged in the PD area. The PD pixel amount is 232,960. PD area covers 92.4% of full size (4672 x 3504).

figure 3-7 PD pixel arrangement



The full size PD pattern is an area of 32x32, evenly placed in the PD area.

figure 3-8 PD pattern



note 1 first 32x32 pattern location is (96, 88) for 4672 x 3504

note 2 PD pixel is on B location but it is a C (clear) pixel

note 3 output image is non-mirrored, non-flipped (0x3821[2]=1)

4 image sensor core digital functions

4.1 mirror and flip

The OV16880 provides mirror and flip readout modes, which respectively reverse the sensor data readout order horizontally and vertically (see **figure 4-1**).

figure 4-1 mirror and flip samples

original image | mirrored image | flipped image | mirrored and flipped image

16880_DS_4_1

table 4-1 mirror and flip registers

address	register name	default value	R/W	description
0x3820	FORMAT1	0x00	RW	Timing Control Register Bit[6]: Vertical flip black lines enable 0: Normal 1: Vertical flip Bit[2]: Array vertical flip enable 0: Normal 1: Vertical flip
0x3821	FORMAT2	0x00	RW	Timing Control Register Bit[2]: Horizontal mirror control 0: Mirrored image 1: Normal image
0x4000	BLC	0x00	RW	BLC Control Register Bit[6]: Vertical flip black lines enable 0: Normal 1: Vertical flip

4.2 image cropping/windowing

An image cropping area is defined by four parameters, horizontal start (HS), horizontal end (HE), vertical start (VS), and vertical end (VE). By properly setting the parameters, any portion within the sensor array size can output as a visible area. When cropping window is adjusted, the sensor timing is also changed. A smaller cropping size in the vertical direction may get a higher frame rate.

Windowing, which is defined by H_win_off and V_win_off, is achieved by masking off the pixels outside of the window; thus, the original timing is not affected.

figure 4-2 image cropping/windowing

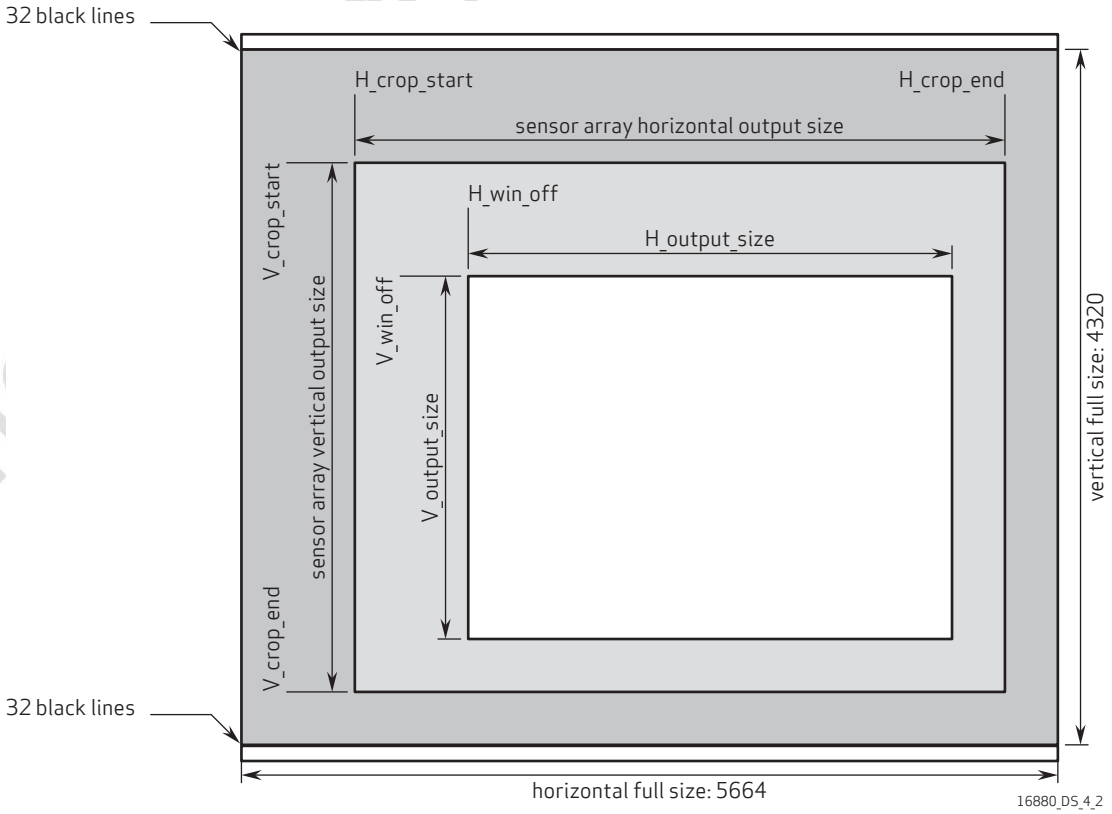


table 4-2 image cropping/windowing control functions (sheet 1 of 2)

address	register name	default value	R/W	description
0x3800	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[15:8] Array horizontal start point
0x3801	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[7:0] Array horizontal start point
0x3802	Y ADDR START	0x04	RW	Bit[7:0]: y_addr_start[15:8] Array vertical start point
0x3803	Y ADDR START	0x00	RW	Bit[7:0]: y_addr_start[7:0] Array vertical start point
0x3804	X ADDR END	0x08	RW	Bit[7:0]: x_addr_end[15:8] Array horizontal end point
0x3805	X ADDR END	0x8B	RW	Bit[7:0]: x_addr_end[7:0] Array horizontal end point
0x3806	Y ADDR END	0x0C	RW	Bit[7:0]: y_addr_end[15:8] Array vertical end point
0x3807	Y ADDR END	0x43	RW	Bit[7:0]: y_addr_end[7:0] Array vertical end point
0x3808	X OUTPUT SIZE	0x10	RW	Bit[7:0]: x_output_size[15:8] ISP horizontal output width
0x3809	X OUTPUT SIZE	0x80	RW	Bit[7:0]: x_output_size[7:0] ISP horizontal output width
0x380A	Y OUTPUT SIZE	0x0C	RW	Bit[7:0]: y_output_size[15:8] ISP vertical output height
0x380B	Y OUTPUT SIZE	0x30	RW	Bit[7:0]: y_output_size[7:0] ISP vertical output height
0x380C	TIMING_HTS	0x12	RW	Bit[7:0]: Horizontal total size[15:8]
0x380D	TIMING_HTS	0xC0	RW	Bit[7:0]: Horizontal total size[7:0]
0x380E	TIMING_VTS	0x0D	RW	Bit[6:0]: Vertical total size[14:8]
0x380F	TIMING_VTS	0x00	RW	Bit[7:0]: Vertical total size[7:0]
0x3810	H_WIN_OFF	0x00	RW	Bit[3:0]: Manual horizontal windowing offset[11:8]
0x3811	H_WIN_OFF	0x04	RW	Bit[7:0]: Manual horizontal windowing offset[7:0]
0x3812	ISP Y WIN	0x00	RW	Bit[7:0]: isp_y_win[15:8] ISP vertical windowing offset
0x3813	ISP Y WIN	0x04	RW	Bit[7:0]: isp_y_win[7:0] ISP vertical windowing offset

table 4-2 image cropping/windowing control functions (sheet 2 of 2)

address	register name	default value	R/W	description
0x3814	H_INC	0x11	RW	Bit[7:4]: Horizontal sub-sample odd increase number Bit[3:0]: Horizontal sub-sample odd increase number
0x3815	H_INC	0x11	RW	Bit[7:4]: Vertical sub-sample odd increase number Bit[4:0]: Vertical sub-sample even increase number

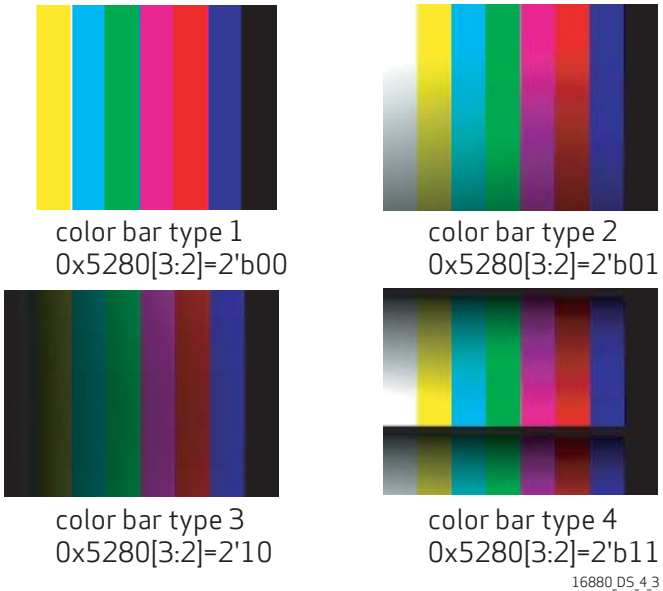
4.3 test pattern

For testing purposes, the OV16880 offers three types of test patterns: color bar, square and random data. The OV16880 also offers two digital effects: transparent effect and rolling bar effect. The output type of digital test pattern is controlled by the test_pattern_type register (0x5280[1:0]). The digital test pattern function is controlled by register 0x5280[7].

4.3.1 color bar

There are four types of color bars which are switched by bar-style in register 0x5280[3:2] (see **figure 4-3**).

figure 4-3 color bar types



color bar type 1
0x5280[3:2]=2'b00

color bar type 2
0x5280[3:2]=2'b01

color bar type 3
0x5280[3:2]=2'10

color bar type 4
0x5280[3:2]=2'b11

16880_DS_4_3

4.3.2 square

There are two types of squares: color square and black-white square. The squ_bw register bit (0x5280[4]) determines which type of square will be output.

figure 4-4 color, black and white square bars

color square　　black-white square

16880_DS_4_4

4.3.3 random data

There are two types of random data test patterns controlled by register 0x5281[4]: frame-changing and frame-fixed random data.

4.3.4 transparent effect

The transparent effect is enabled by transparent_en register (0x5280[5]). If this register is set, the transparent test pattern will be displayed. The following image is an example showing a transparent color bar image (see **figure 4-5**).

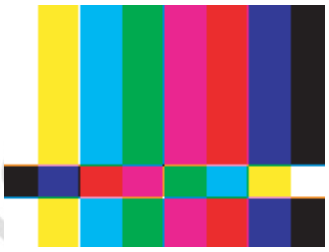
figure 4-5 transparent effect

16880_DS_4_5

4.3.5 rolling bar effect

The rolling bar is set by rolling_bar_en register (0x5280[6]). If it is set, an inverted-color rolling bar will roll from up to down. The following image is an example showing a rolling bar on color bar image (see **figure 4-6**).

figure 4-6 rolling bar effect



16880_DS_4_6

table 4-3 test pattern registers

address	register name	default value	R/W	description
0x5280	PRE CTRL00	0x00	RW	Bit[7]: Test pattern enable Bit[6]: Rolling bar function enable Bit[5]: Transparent enable 0: Disable transparent effect function 1: Enable transparent effect function Bit[4]: Square mode 0: Color square 1: Black-white square Bit[3:2]: Color bar style 00: Standard color bar 01: Top-bottom darker color bar 10: Right-left darker color bar 11: Bottom-top darker color bar Bit[1:0]: Test pattern mode 00: Color bar 01: Random data 10: Square pattern 11: Black image
0x5281	PRE CTRL01	0x41	RW	Bit[6]: Window cut enable 0: Do not cut the redundant pixels 1: Cut the redundant pixels Bit[5]: two_lsb_0_en When set, two LSBs of output data are 0 Bit[4]: Same seed enable When set, the seed used to generate the random data are same which is set in seed register Bit[3:0]: Random seed Seed used in generating random data

4.4 black level calibration (BLC)

The pixel array contains several optically shielded (black) lines. These lines are used as reference for black level calibration.

There are two main functions of the BLC:

- applying all normal pixel values based on the values of the black levels
- applying multiplication to all the pixel values based on digital gain

table 4-4 BLC control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x11	RW	Bit[7]: Debug mode Bit[6]: Vertical flip black lines enable 0: Normal 1: Vertical flip Bit[5]: Debug mode Bit[4]: r_dc_man Set 1-channel BLC DC offset manually Bit[3]: target_adj_dis Disable adjust final applied target Bit[2]: cmp_en Compensation enable by adding color channel difference when using 1-channel BLC Bit[1]: dither_en Dithering enable Bit[0]: mf_en Median filter enable
0x4001	BLC CTRL01	0x40	RW	Bit[7:6]: Debug mode Bit[5]: kcoef_man_en Set dark current coefficient manually Bit[4]: off_man_en Set BLC offset manually Bit[3]: zero_ln_out_en Zero line output enable Bit[2]: blk_ln_out_en Black line output enable Bit[1:0]: byp_mode No black offset will be applied on image
0x4002	BLK LVL TARGET	0x00	RW	Bit[7:2]: Not used Bit[1:0]: blk_lvl_target[9:8] BLC target high 2 bits
0x4003	BLK LVL TARGET	0x10	RW	Bit[7:0]: blk_lvl_target[7:0] BLC target low 8 bits

table 4-4 BLC control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x4004	HWIN OFF	0x00	RW	Bit[7:4]: Not used Bit[3:0]: hwin_off[11:8] Left boundary of BLC window high 4 bits
0x4005	HWIN OFF	0x04	RW	Bit[7:0]: hwin_off[7:0] Left boundary of BLC window low 8 bits
0x4006	HWIN PAD	0x00	RW	Bit[7:4]: Not used Bit[3:0]: hwin_pad[11:8] Right boundary of BLC window high 4 bits
0x4007	HWIN PAD	0x04	RW	Bit[7:0]: hwin_pad[7:0] Right boundary of BLC window low 8 bits
0x400A	OFF LIM TH	0x02	RW	Bit[7:0]: off_lim_th[15:8] Threshold for the difference between difference channels in the same frame high 8 bits (works only when register 0x4000[3] = 0)
0x400B	OFF LIM TH	0x00	RW	Bit[7:0]: off_lim_th[7:0] Threshold for the difference between difference channels in the same frame low 8 bits (works only when register 0x4000[3] = 0)
0x400F	BLC CTRL0F	0x80	RW	Bit[7]: r_exp_chg_trig_en Exposure BLC trigger enable
0x4010	BLC CTRL10	0xF0	RW	Bit[7]: off_trig_en Offset BLC trigger enable Bit[6]: gain_chg_trig_en Gain change BLC trigger enable Bit[5]: fmt_chg_trig_en Format change BLC trigger enable Bit[4]: rst_trig_en Reset BLC trigger enable Bit[3]: man_avg_en BLC average in V BLC manual trigger (works only when register 0x4010[2] = 1) Bit[2]: man_trig Manual BLC trigger enable Bit[1]: off_frz_en BLC freeze enable Bit[0]: off_always_up BLC always update enable
0x4012	BLC CTRL12	0x08	RW	Bit[7:0]: rst_trig_fn Number of BLC update frames with reset trigger

table 4-4 BLC control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x4013	BLC CTRL13	0x02	RW	Bit[7:0]: fmt_trig_fn Number of BLC update frames with format change trigger
0x4014	BLC CTRL14	0x02	RW	Bit[7:0]: gain_trig_fn Number of BLC update frames with gain change trigger
0x4015	BLC CTRL15	0x02	RW	Bit[7:0]: off_trig_fn Number of BLC update frames with offset trigger
0x4016	OFF TRIG TH	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_trig_th[9:8] Threshold of offset trigger high 2 bits
0x4017	OFF TRIG TH	0x04	RW	Bit[7:0]: off_trig_th[7:0] Threshold of offset trigger low 8 bits

4.5 one time programmable (OTP) memory

The OV16880 supports a maximum of 2560 bytes of one-time programmable (OTP) memory to store chip identification and manufacturing information, which can be used to update the sensor's default setting and can be controlled through the SCCB (see **table 4-6**). OTP data can be accessed using registers 0x7000~0x79FF through the SCCB interface. Registers 0x7010~0x768F (1664 bytes total) are reserved for customer use and the rest of the OTP memory (0x7000~0x700F and 0x7690~0x79FF) are reserved for OmniVision.

table 4-5 OTP allocation

start address	end address	byte usage	assignment	byte type
0x7000	0x700F	16	reserved for OmniVision	DATA
0x7010	0x768F	1664	reserved for customer	DATA
0x7690	0x79FF	880	reserved for OmniVision	DATA
0x7000	0x79FF	2560	total	DATA

4.5.1 OTP procedure

When accessing sensor OTP, disable sensor OTP cluster cancellation function by setting register bit 0x5000[0] = 0. The OTP operation is related to the system clock. The following settings are based on a 24 MHz input clock. Please contact your local OmniVision FAE, when using an alternate input clock.

Set PLL and start streaming before write or read:

```
PLL setting
6C 0100 01
20ms delay required
```

To write OTP (for example, write 0x01 to 0x7000):

```
6C 7000 01
6C 3D84 40
6C 3D88 00
6C 3D89 00
6C 3D8A 00
6C 3D8B 00
6C 3D80 01
200ms delay required
6C 3D80 00
```

Registers {0x3D88, 0x3D89} are the program start address. Registers {0x3D8A, 0x3D8B} are the program end address. The address range is from 0 to 0x9FF. The corresponding registers are from 0x7000 to 0x79FF.

To read OTP (for example, read 0x7000):
If reading the same OTP after write, it will return the register value that was written even if it fails. So it can be read after power off/ power on or after writing the register with a different value first.

```
6C 3D81 01
20ms delay required
Read register 0x7000
```

4.5.2 OTP other functions

OTP loading data can be triggered when powering up or writing 0x01 to register 0x3D81. Power up loading data is enabled by register 0x3D85[2], by default it is off. Auto mode and manual mode can be chosen by setting register 0x3D84[6] to 0 and 1, respectively, and by default, it is in auto mode. In auto mode, all data in the OTP will be loaded to the OTP buffer; while in manual mode, part of the data which is defined by the start address ({0x3D88,0x3D89}) and the end address ({0x3D8A, 0x3D8B}) of the OTP will be loaded to the OTP buffer.

The OTP memory access conditions are based on typical conditions: sensor wakeup, 2.8~3.0V AVDD, 1.2V DVDD, and 144 MHz system clock.

Set register bit 0x5000[0] to "0" before any OTP access to avoid timing conflict which may cause OTP read/write failure. After OTP access is complete, set register bit 0x5000[0] back to "1".

To use OTP memory under different operating conditions, please contact your local OmniVision FAE.

table 4-6 OTP control registers

address	register name	default value	R/W	description
0x3D80	OTP_PROGRAM_CTRL	0x00	RW	Bit[7]: OTP_wr_busy (read only) Bit[0]: OTP_program_enable (write only)
0x3D81	OTP_LOAD_CTRL	0x00	RW	Bit[7]: OTP_rd_busy (read only) Bit[5]: OTP_bist_error (read only) Bit[4]: OTP_bist_done (read only) Bit[0]: OTP_load_enable
0x3D84	OTP_MODE_CTRL	0x00	RW	Bit[7]: Program disable 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode
0x3D85	OTP_REG85	0x13	RW	Bit[5]: OTP_bist_select 0: Compare with SRAM 1: Compare with zero Bit[4]: OTP_bist_enable Bit[2]: OTP power up load data enable Bit[1]: OTP power up load setting enable Bit[0]: OTP write register load setting enable
0x3D88	OTP_START_ADDRESS	0x00	RW	OTP Start High Address for Manual Mode
0x3D89	OTP_START_ADDRESS	0x00	RW	OTP Start Low Address for Manual Mode
0x3D8A	OTP_END_ADDRESS	0x00	RW	OTP End High Address For Manual Mode
0x3D8B	OTP_END_ADDRESS	0x00	RW	OTP End Low Address For Manual Mode
0x3D8C	OTP_SETTING_STT_ADDRESS	0x00	RW	OTP Start High Address For Load Setting
0x3D8D	OTP_SETTING_STT_ADDRESS	0x00	RW	OTP Start Low Address For Load Setting
0x7000~0x79FF	OTP_SRAM	0x00	RW	Bit[7:0]: OTP buffer

4.6 temperature sensor

The OV16880 supports an on-chip temperature sensor that covers -64° ~ +192°C with an error up to 5°C. It can be controlled through the SCCB interface (see **table 4-7**).

If {0x4D13, 0x4D14} ≤ 0xC000, the temperature is positive, T_J(°C) = {0x4D13, 0x4D14}/256. If {0x4D13, 0x4D14} > 0xC001, temperature is negative, T_J(°C) = {0x4D13[5:0], 0x4D14}/256.

Before reading the temperature, the temperature sensor should be triggered by a 0 to 1 transition of register 0x4D12[0].

table 4-7 temperature sensor functions

address	register name	default value	R/W	description
0x4D12	TPM_CTRL_12	–	W	Writing 0x4D12[0] to '1' will trigger temperature calculation, then 0x4D12 and 0x4D13 will be latched temperature value
0x4D13	TPM_CTRL_13	–	R	Latched Temperature Value, Integer Part
0x4D14	TPM_CTRL_14	–	R	Latched Temperature Value, Decimal Part

4.7 strobe flash and frame exposure

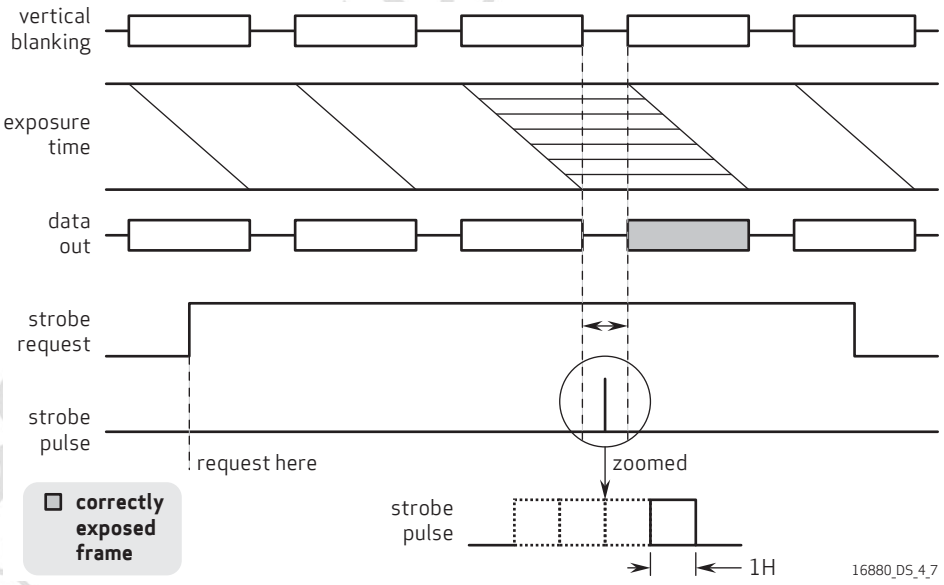
4.7.1 strobe flash control

The strobe signal is programmable using register 0x3B00[2:0]. It supports both LED and Xenon modes. The polarity of the pulse can be changed. The strobe signal is enabled (turned high/low depending on the pulse's polarity) by requesting the signal via the SCCB interface. Flash modules are triggered by the rising edge by default or by the falling edge if the signal polarity is changed. The OV16880 supports the following flashing modes: xenon flash control, LED mode 1, LED mode 2, LED mode 3, and LED mode 4.

4.7.1.1 xenon flash control

After a strobe request is submitted, the strobe pulse will be activated at the beginning of the third frame (see **figure 4-7**). The third frame will be correctly exposed. The pulse width can be changed in Xenon mode between 1H and 4H controlled by register 0x3B00[5:4], where H is one row period.

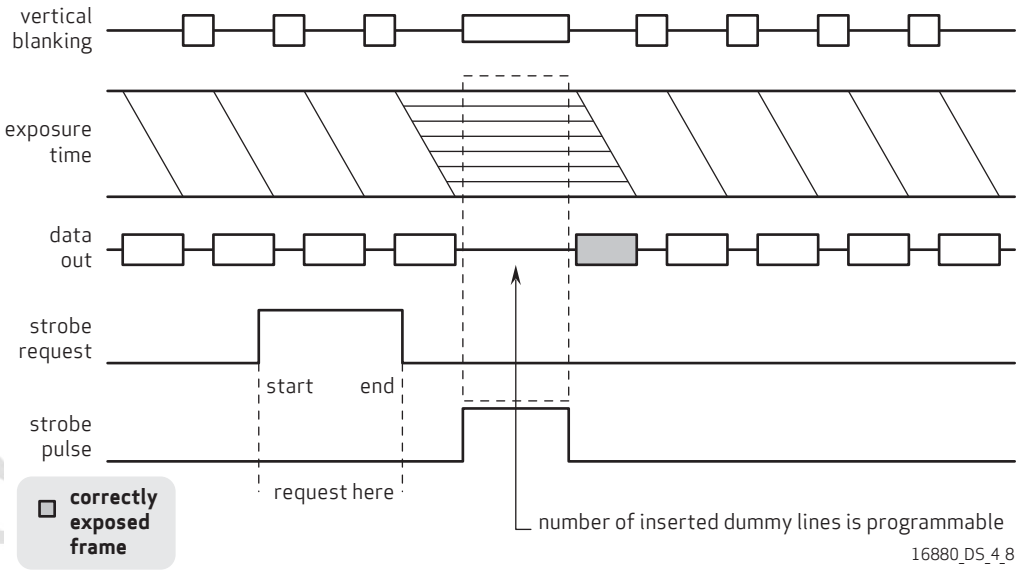
figure 4-7 xenon flash mode



4.7.1.2 LED 1 & 2 mode

In LED 1 & 2 modes, the strobe pulse is active two frames after the strobe request is submitted and the third frame is correctly exposed. The strobe pulse will be activated only one time if the strobe end request is set as shown in **figure 4-8**. If end request has not been sent, the strobe signal is activated intermittently until the strobe end request is set (see **figure 4-9**). The strobe width is programmable.

figure 4-8 LED 1 & 2 mode - one pulse output

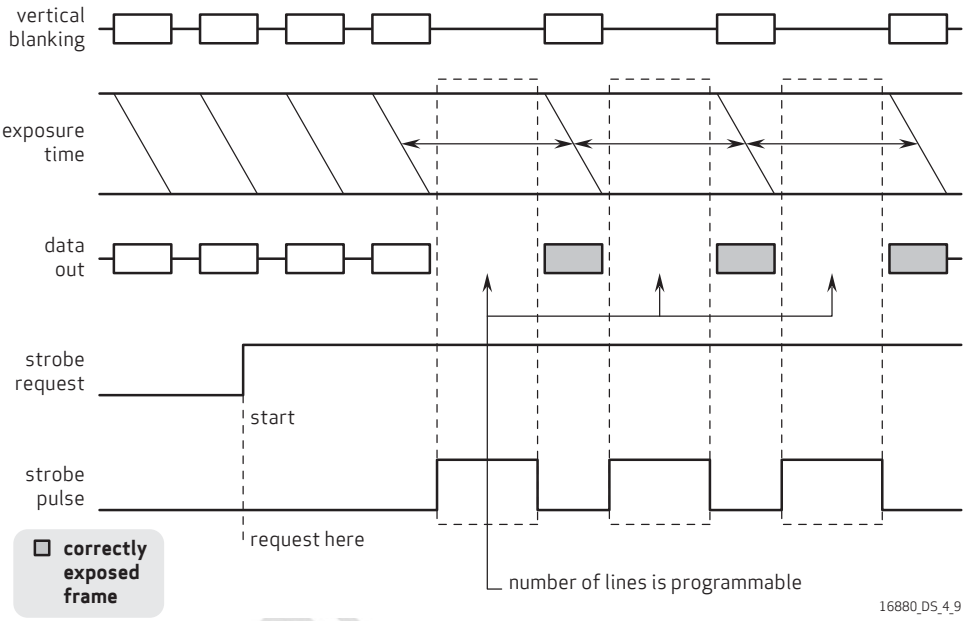


The strobe width is controlled by registers 0x3B02 and 0x3B03. The inserted dummy lines are used for the additional exposure lines added to 0x3501~0x3502. The maximum line of 0x3B02 and 0x3B03 is calculated by 0x7FFF0 - {0x3501, 0x3502}.

Example of LED 1 & 2 mode:

```
20 3b00 01 ;Select led 1 mode
20 3b02 00 ;Set strobe width
20 3b03 3f ;Set strobe width
20 3002 80 ;Set the VSYNC output enable
20 3b00 81 ;Request on
;delay 100 ;if using LED 2 mode
20 3b00 00 ;Request off
```

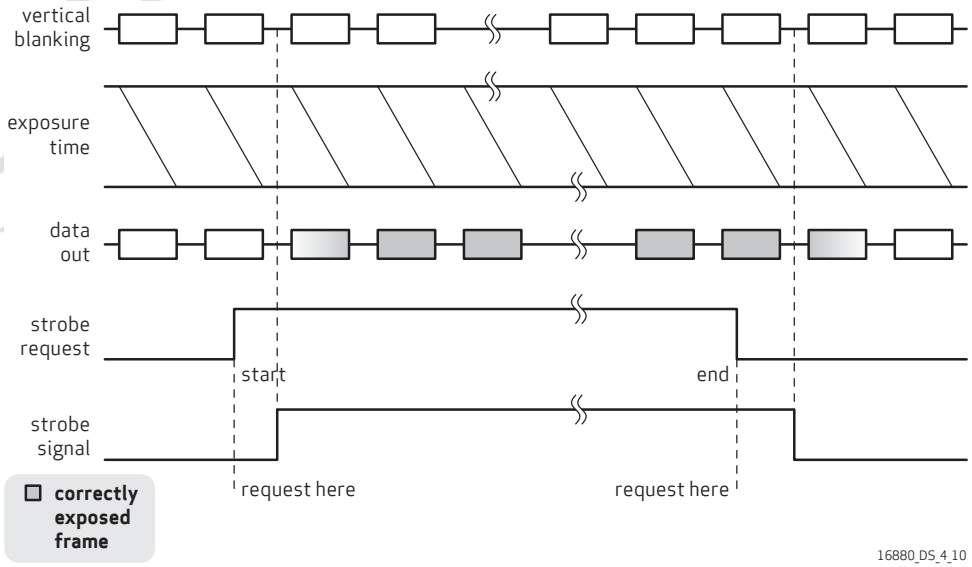
figure 4-9 LED 1 & 2 mode - multiple pulse output



4.7.1.3 LED 3 mode

In LED 3 mode, the strobe signal stays active until the strobe end request is sent (see **figure 4-10**).

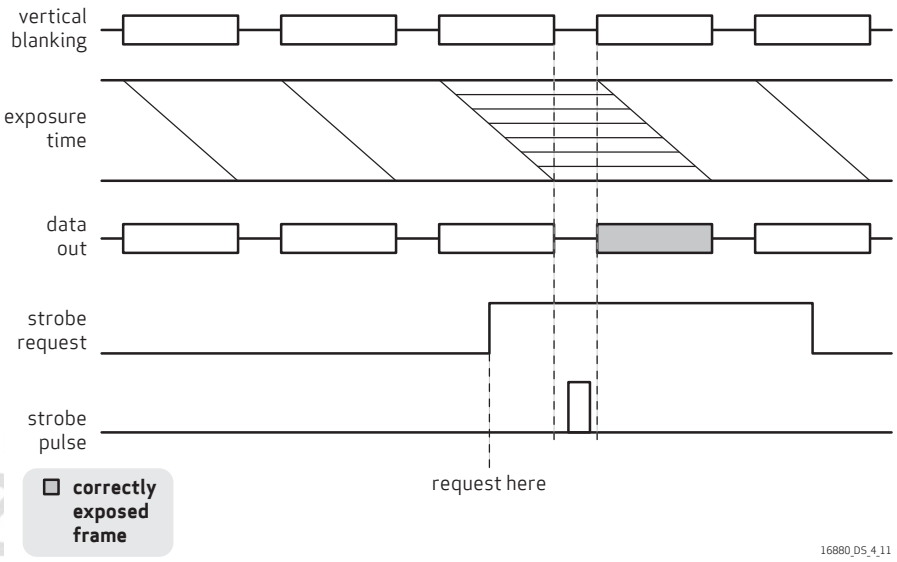
figure 4-10 LED 3 mode



4.7.1.4 LED 4 mode

In LED 4 mode, the strobe signal width is controlled by register 0x3B05 (see **figure 4-11**). Strobe width = 128 × (2^0x3B05[1:0]) × (0x3B05[7:2] + 1) × sclk_period. The maximum value of 0x3B05[7:2] is 6'b111110.

figure 4-11 LED 4 mode



4.7.2 frame exposure (FREX) mode

In FREX mode, all pixels in the frame start integration at the same time, rather than integrating row by row. After a user-defined exposure time, the mechanical shutter should be closed, preventing further integration, and then the image begins to read out. After the readout finishes, the shutter opens again and the sensor resumes normal mode, waiting for the next FREX request.

The OV16880 supports two modes of FREX (see **figure 4-12** and **figure 4-13**):

figure 4-12 FREX mode 1

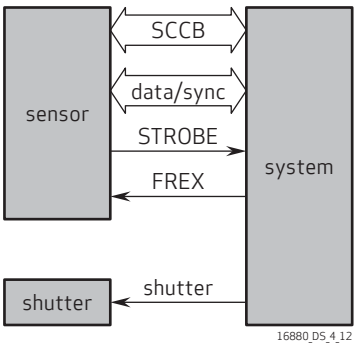
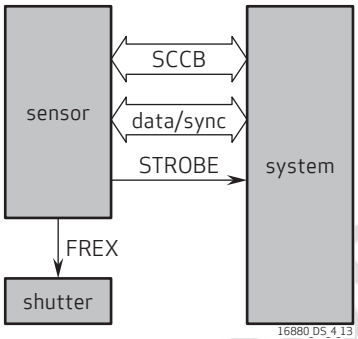


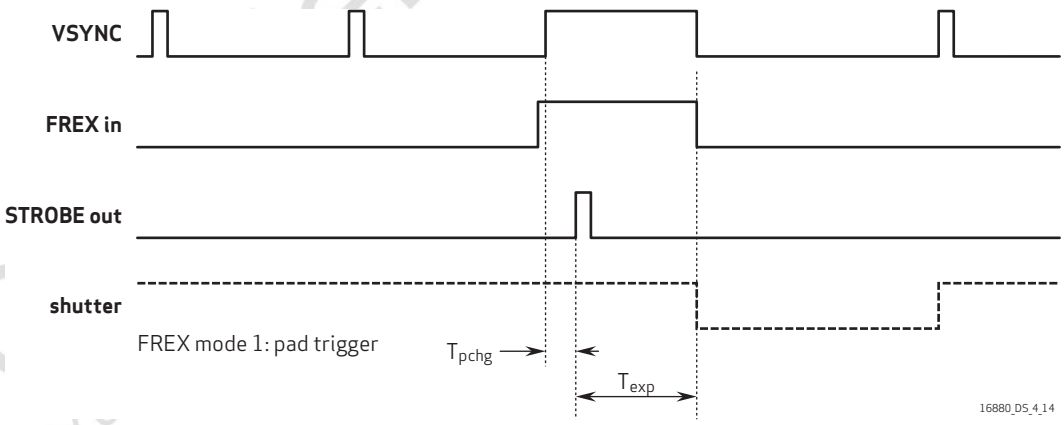
figure 4-13 FREX mode 2



In mode 1, the FREX pin is configured as an input while it is configured as an output in mode 2. In both mode 1 and mode 2, the strobe output is irrelevant with the rolling strobe function. When in rolling shutter mode, the strobe function and this FREX/shutter control function do not work at the same time.

The timing diagram for mode 1 is shown in **figure 4-14**.

figure 4-14 FREX mode 1 timing diagram



In mode 1, the host asserts FREX at any time in preview mode (mechanical shutter is open at this time). The sensor will trigger STROBE to indicate the start of exposure time. Exposure time is calculated from the STROBE rising edge to when the mechanical shutter closes. The host will control when to close the mechanical shutter (shutter delay is handled by the host). The host can re-open the shutter after receiving the entire image data or the next VSYNC signal.

The timing diagram for mode 2 is shown in **figure 4-15** and **figure 4-16**.

figure 4-15 FREX mode 2 (shutter delay = 0) timing diagram

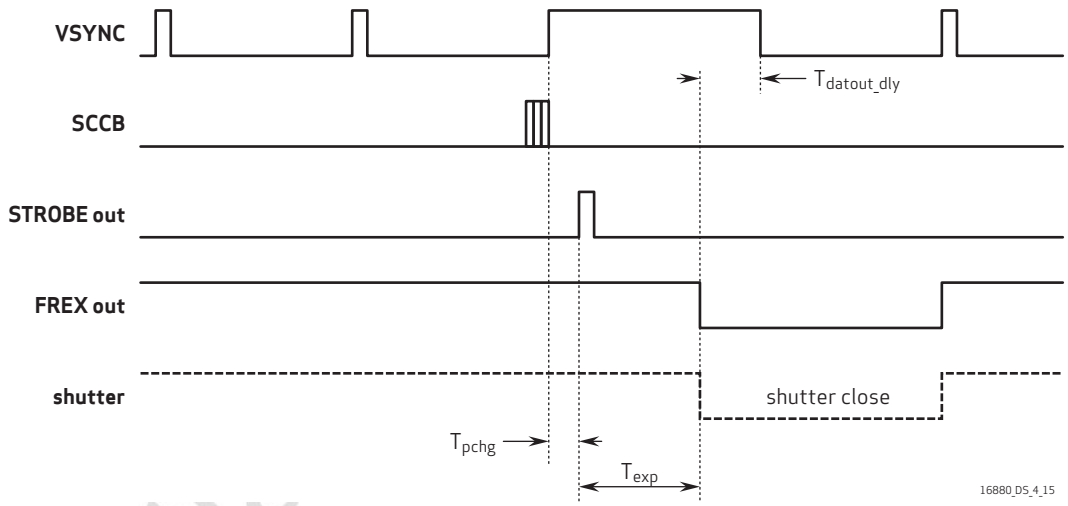
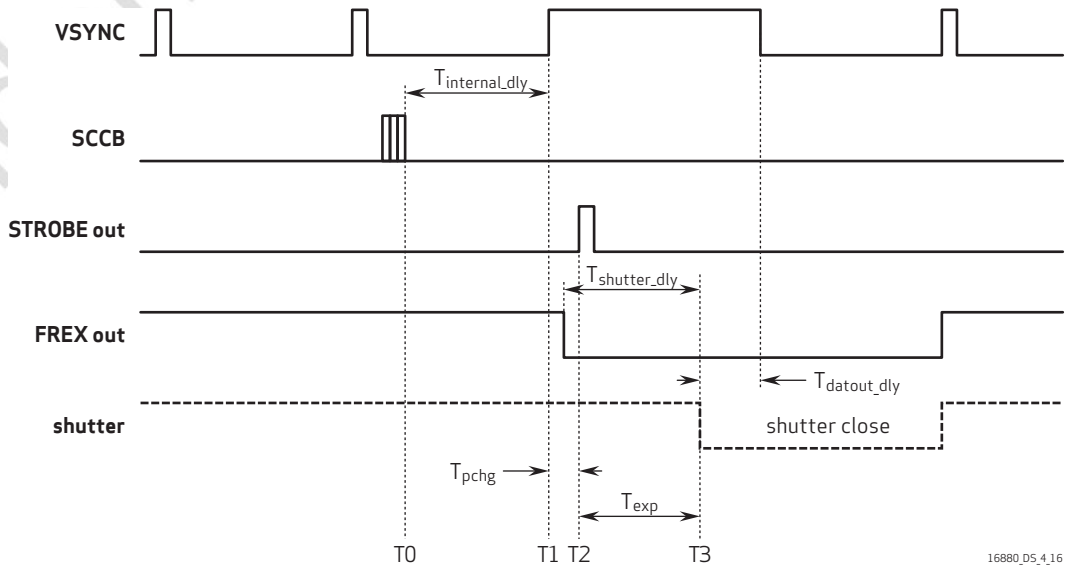


figure 4-16 FREX mode 2 (shutter delay > 0) timing diagram



Before using mode 2, the host needs to program exposure time (registers 0x3F85, 0x3F86, 0x3F87), shutter delay (registers 0x3F8C, 0x3F8D), strobe width (registers 0x3F89, 0x3F8A, 0x3F8B), and data output delay. The host triggers this mode by SCCB at any time in preview mode (mechanical shutter is open at this time). The sensor can either start frame exposure right away (since the current data packet is broken, the receiver may get a packet error) or wait for the current frame to finish (controlled by register 0x3F9F[0]). If there is no STROBE delay, the sensor will trigger STROBE to indicate the start of exposure time. Exposure time is calculated from STROBE rising edge to when the mechanical shutter closes. Otherwise, the STROBE signal will be sent out even before the sensor begins to pre-charge. The host can control the sensor to start sending image data after a certain delay (registers 0x3F90, 0x3F91) after FREX goes low. The host can re-open the shutter after receiving the entire image data or the next VSYNC signal.

See **table 4-8** for FREX strobe control functions.

table 4-8 flash strobe control registers

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Bit[7]: Strobe ON/OFF Bit[6]: Strobe polarity 0: Active high 1: Active low Bit[5:4]: width_in_xenon Bit[2:0]: Strobe mode 000: Xenon 001: LED1 010: LED2 011: LED3 100: LED4
0x3B02	STROBE DMY H	0x00	RW	Bit[7:0]: strobe_add_dummy[15:8] Dummy line number added at strobe high byte
0x3B03	STROBE DMY L	0x00	RW	Bit[7:0]: strobe_add_dummy[7:0] Dummy line number added at strobe low byte
0x3B04	STROBE CTRL	0x00	RW	Bit[7:4]: Not used Bit[3]: start_point_sel Bit[2]: Strobe repeat enable Bit[1:0]: Strobe latency 00: Strobe generated at next frame 01: Delay one frame Strobe generated 2 frames later 10: Delay one frame Strobe generated 3 frames later 11: Delay one frame Strobe generated 4 frames later
0x3B05	STROBE WIDTH	0x00	RW	Bit[7:2]: Strobe pulse width step Bit[1:0]: Strobe pulse width gain strobe_pulse_width = 128×(2^gain)×(step+1)×Tsclk

table 4-9 FREX strobe control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3F85	FREX REG5	0x08	RW	Bit[7:0]: Frame exposure[23:16] MSB of frame exposure time in mode 2 Exposure time in units of 128 system clock cycles
0x3F86	FREX REG6	0x00	RW	Bit[7:0]: Frame exposure[15:8] Middle byte of frame exposure time in mode 2
0x3F87	FREX REG7	0x08	RW	Bit[7:0]: Frame exposure[7:0] LSB of frame exposure in mode 2
0x3F89	FREX REG9	0x00	RW	Bit[3:0]: strobe_width[19:16] MSB of strobe width in mode 2. Strobe width in units of 1 system clock cycle
0x3F8A	FREX REGA	0x06	RW	Bit[7:0]: strobe_width[15:8] Middle byte of strobe width in mode 2
0x3F8B	FREX REGB	0x00	RW	Bit[7:0]: strobe_width[7:0] LSB of strobe width in mode 2
0x3F8C	FREX REGC	0x00	RW	Bit[4:0]: shutter_dly[12:8] MSB of shutter delay in mode 2 Shutter delay is in units of 128 system clock cycles
0x3F8D	FREX REGD	0x44	RW	Bit[7:0]: shutter_dly[7:0] LSB of shutter delay in mode 2
0x3F8E	FREX REGE	0x1F	RW	Bit[7:0]: frex_pre_charge_width[15:8] MSB of sensor precharge in mode 2 Sensor precharge is in units of 1 system clock cycles
0x3F8F	FREX REGF	0x40	RW	Bit[7:0]: frex_pre_charge_width[7:0] LSB of sensor precharge in mode 2
0x3F90	FREX REG10	0x00	RW	Bit[7:0]: Readout delay[15:8] MSB of readout delay time in mode 2 Readout delay time is in units of 128 system clock cycles
0x3F91	FREX REG11	0x01	RW	Bit[7:0]: Readout delay[7:0] LSB of readout delay time in mode 2
0x3F92	FREX_REG12	0x00	RW	Bit[4:0]: sensor_strobe_dly[12:8] MSB of strobe delay time
0x3F93	FREX_REG13	0x00	RW	Bit[7:0]: Strobe delay[7:0] LSB of strobe delay time

table 4-9 FREX strobe control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3F9E	FREX REG1E	0x01	RW	Bit[0]: frex_sccb_req_repeat_trig_sel 0: SOF 1: EOF
0x3F9F	FREX REG1F	0x04	RW	Bit[7]: frex_sccb_req Self clearing Bit[5]: frex_strobe_out_sel 0: Strobe for rolling mode 1: Strobe for frame mode Bit[4]: frex_nopchg Bit[3]: frex_strobe polarity 0: Active high 1: Active low Bit[2]: frex_shutter polarity 0: Active high 1: Active low Bit[1]: frex_pad_in_enable 0: Frame mode is triggered by register 1: Frame mode is triggered by FREX pad Bit[0]: no_latch at SOF for frex_sccb_req 0: Trigger frame mode in SOF 1: Trigger frame mode immediately

4.7.3 exposure time control

registers: r_frame_exp = {0x3F85, 0x3F86, 0x3F87}, 24 bits, 1 step = 128 clock cycles

minimum exposure time: 0x3F85 = 0x00, 0x3F86 = 0x00, 0x3F87 = 0x00

If the OV16880 works at 160 MHz, the minimum exposure time is 0 and minimum step is 800 ns

maximum exposure time: 0x3F85 = 0xFF, 0x3F86 = 0xFF, 0x3F87 = 0xFF

If the OV16880 works at 160 MHz, the maximum exposure time is 13.42 sec

4.7.4 shutter delay control

registers: r_shutter_dly = {0x3F8C[4:0], 0x3F8D[7:0]}, 13 bits, 1 step = 128 clock cycles

minimum shutter delay time: 0x3F8C = 0x00, 0x3F8D = 0x00

Minimum step is 800 ns.

maximum shutter delay time: 0x3F8C = 0x1F, 0x3F8D = 0xFF.

If the OV16880 works at 160 MHz, the maximum shutter delay time is 6.55 ms.

4.7.5 sensor pre charge control

registers: r_frex_pchg = {0x3F8E[7:0], 0x3F8F[7:0]}, 16 bits, 1 step = 1 system clock cycle

These registers affect sensor performance. It is for internal use and not recommended for customer to change.

4.7.6 strobe control

Registers: r_strobe_width = {0x3F89[3:0], 0x3F8A[7:0], 0x3F8B[7:0]}, 20 bits, 1 step = 1 clock cycle.

These registers control the strobe signal output width.

4.7.6.1 strobe delay control

Registers: r_shutter_dly = {0x3F82[4:0], 0x3F83[7:0]}, 13 bits, 1 step = 256 clock cycles.

Minimum strobe delay time: 0x3F82=0x00, 0x3F83=0x00.

Minimum step is 1.45 µs.

Maximum strobe delay time: 0x3F82=0x1F, 0x3F83=0xFF.

If the OV16880 works at 176 MHz, the maximum strobe delay time is 11.876 ms.

4.7.6.2 data out delay

Registers: r_dataout_dly = {0x3F80[7:0], 0x3F81[7:0]}, 16 bits, 1 step = 256 clock cycles.

Minimum step is 1.52 µs.

Maximum data delay time: 0x3F80 = 0xFF, 0x3F81 = 0xFF

If OV16880 works at 176 MHz, the maximum data out delay time is 99.61 ms.

4.8 embedded line

In the OV16880, embedded line is controlled by firmware, which the user can configure the registers being output in embedded line. One or more rows of embedded data can be output at the beginning or end of image frame. The embedded line number is controlled by register 0x5C08[7:4], the position of the embedded line is controlled by register 0x5C08[2]. In total, embedded line can support up to 2048 bytes of data.

4.8.1 table setup

To configure embedded line, the embedded table must be setup first.

The table format is shown below:

```
byte0: embedded line byte number[15:8]

byte1: embedded line byte number[7:0]

byte2: first group register start address[15:8]

byte3: first group register start address[7:0]

byte4: first group byte number

byte5: second group register start address[15:8]
```

byte6: second group register start address[7:0]

byte7: second group byte number

…

Example: the embedded line table with data from register address 5000 ~ 5010, 3808~3814 is:

6c 9a00 00

6c 9a01 1c

6c 9a02 50

6c 9a03 00

6c 9a04 10

6c 9a05 38

6c 9a06 08

6c 9a07 0c

6c 3907 07

6c 3903 01

6c 3666 01

4.8.2 embedded line output

Embedded line is output in front of image line. Valid embedded line content width is programmable. Invalid embedded line content is fixed and filled with dummy data from one programmable byte. Embedded line supports tag and no tags. Tag value is programmable. Embedded line valid data width should be a multiple of four.

table 4-10 embedded line registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3666	CORE_REG	0x00	RW	Bit[0]: Embedded lines enable at system level
0x3900	REG0	0x00	RW	Bit[7:6]: Reserved Bit[5]: Embedded line done interrupt clear bit Writing 1 will clear embedded line done interrupt. Writing 0 does not change status Bit[4]: SRAM violation interrupt clear bit Writing 1 will clear SRAM violation interrupt. Writing 0 does not change status Bit[3]: Embedded line done interrupt status bit Bit[2]: SRAM violation interrupt status bit Bit[1]: Embedded line done interrupt enable Bit[0]: SRAM violation interrupt enable

table 4-10 embedded line registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3901	REG1	0xFF	RW	Bit[7:0]: Dummy data value which will appear on image data bus when embedded line reach the length specified by registers {0x3906, 0x3907}
0x3902	REG2	0xAD	RW	Bit[7:0]: Tag value
0x3903	REG3	0x00	RW	Bit[7:3]: Reserved Bit[2]: One of this bit indicates embedded line is active Bit[1]: Tag data insertion enable bit Bit[0]: Embedded line function enable bit
0x3906	REG6	0x00	RW	Bit[7:0]: Embedded lines total length low byte Tag data are not included in this total length
0x3907	REG7	0x00	RW	Bit[7:0]: Embedded lines total length low byte Tag data are not included in this total length
0x5C08	WIN MAN EN	0x00	RW	Bit[7:4]: Embedded line number Bit[2]: Embedded line position 0: At beginning of image frame 1: At end of image frame

5 image sensor processor digital functions

5.1 DSP general description

The OV16880 ISP supports 1-exposure and 2-exposure sensor.

Following work modes are supported:

- normal 1-exposure mode
- 2-exposure mode quarter-size DCW
- 2-exposure mode quarter-size binning

5.2 ISP block diagram

A simple ISP block diagram is shown in **figure 5-1**. RAW_PROCESS includes some essential modules for RAW image process, such as LENC, DPC, and etc. HDR_PROCESS combines multiple exposure images into a single one with high dynamic range.

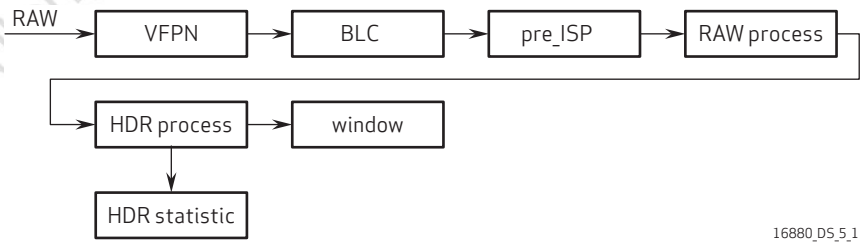
Exposure mode can be configured from system control register. It can also be configured manually by register.

- 0x5004[5:4]: 2'b00: non-HDR (default), 2'b01: 2-expo
- 0x5005[0]: 0: auto exposure mode, exposure mode defined by 0x3821[7:6], 1: manual exposure mode, exposure mode defined by register 0x5004[5:4]

If the first pixel's exposure changes (cropped, mirrored or flipped), the HDR pattern can be set by:

- 0x5004[3:2]: 2'b00: begin with long, 2'b01: begin with short
- 0x5000[2]: LENC enable
- 0x5000[1]: AWB_gain enable
- 0x5000[0]: OTP enable
- 0x5001[6]: DPC enable

figure 5-1 ISP block diagram



5.3 DCW

The DCW module is used to down scale raw images in horizontal (X) or/and vertical (Y) direction. In different work modes, the x or y direction dump scale may be enabled/disabled separately:

- 2 exposure HDR (quarter size output): X dump scale is enabled when no binning operation has been preformed; Y dump scale is disabled.
- Non HDR: X and Y dump scale are both enabled, and scale bits can be any value between 0~3

Scale bits can be 0~3, and different sizes will be required:

- 0: No scale, X/Y size must be a multiple of 2
- 1: 1/2 size dump scale, X/Y size must be a multiple of 8
- 2: 1/4 size dump scale, X/Y size must be a multiple of 16
- 3: 1/8 size dump scale, X/Y size must be a multiple of 32

The scale ratio can be configured from the system or can be manually set by:

- 0x5006[5]: manual mode enable
- 0x501D[7:6]: manual value of horizontal down scale ratio
- 0x501D[5:4]: manual value of vertical down scale ratio

5.4 LENC

LENC corrects the lens shading due to light fall off in the corner areas. It computes a gain pixel by pixel according to G/B/R control points matrix (control registers). Then, it applies the gain to each pixel in the image. The G, B, R control point matrix sizes are 16x16 each.

Control points are selected according to the absolute coordinate of the input pixel in the sensor array. If y_offset and x_offset are not 0, the control point may not be selected from (0,0). Also, if the image is flipped, it will select control point from the end.

A parameter m_nQ is used to adjust gain for the pixel. It can be auto calculated from the real gain or be manually set.

figure 5-2 lens correction graph

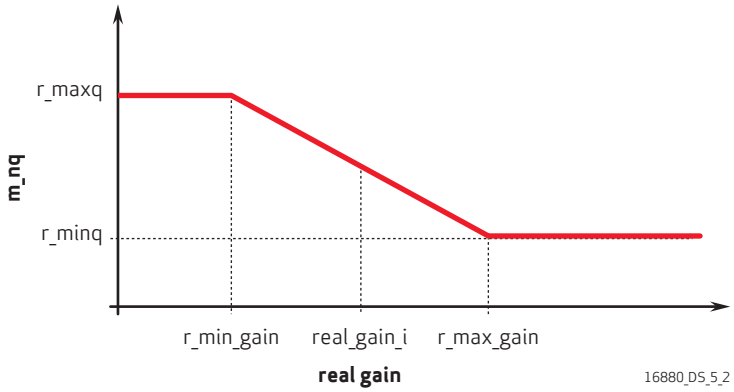


table 5-1 lens correction register

address	register name	default value	R/W	description
0x2800~ 0x28FF	COEFFICIENT FOR G CHANNEL	0x80	RW	Coefficient for G channel
0x2900~ 0x29FF	COEFFICIENT FOR B CHANNEL	0x80	RW	Coefficient for B channel
0x2A00~ 0x2AFF	COEFFICIENT FOR R CHANNEL	0x80	RW	Coefficient for R channel
0x2B00	MAXGAIN	0x60	RW	Bit[7:0]: Maxgain[7:0]
0x2B01	MINGAIN	0x40	RW	Bit[7:0]: Mingain[7:0]
0x2B02	MAXQ	0x40	RW	Bit[7:0]: Maxq[7:0]
0x2B03	MINQ	0x18	RW	Bit[7:0]: Minq[7:0]
0x2B04	LENC_CTRL	0x36	RW	Bit[2]: Lens correction control 0: Manually set Q value by register 0x2B02 1: Calculate Q according to real_gain
0x2B05	HSCALE	0x01	RW	Bit[7:5]: Not used Bit[4:0]: hscale[12:8]
0x2B06	HSCALE	0xE1	RW	Bit[7:0]: hscale[7:0]
0x2B07	VSCALE	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Vscale[12:8]
0x2B08	VSCALE	0x41	RW	Bit[7:0]: Vscale[7:0]
0x2B09	R LENC CTRL1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: dither_g[3:0]

5.5 defect pixel cancellation (DPC)

The main purpose of the DPC function is to remove white and black defective pixels. If the pixel is defective, DPC will use a value calculated from the neighboring normal pixels to replace it.

In DPC control, the different type of clusters and correction criteria with gain change can be programmed by registers 0x5600~0x567A.

5.6 white balance

The RAW R/G/B values of a gray object vary with the spectrum of the illumination and the sensor spectral response. The illumination spectrum is usually described by "color temperature", which is the surface temperature of a black body radiating equivalent spectrum. In the real world, the light color temperature ranges from very low (reddish) to very high (bluish) value. For example, the color temperature of an incandescent lamp is about 2850K, while the color temperature of an overcast day is about 6500K.

To make sure that a gray image is truly gray, the sensor needs to adjust the gain for each color channel according to color temperature. This process is called white balance (WB).

White balance gain is enabled by default and can be disabled in register 0x5000[1]. The applied WB gain and offset values can be read back from or set into registers 0x5300~0x5316 (long exposure), and 0x5340~0x5356 (short exposure).

table 5-2 gain and offset chart

exposure	gain				offset			
	B	Gb	Gr	R	B	Gb	Gr	R
long	{0x5300, 0x5301}	{0x5302, 0x5303}	{0x5304, 0x5305}	{0x5306, 0x5307}	{0x5308, 0x5309, 0x530A}	{0x530C, 0x530D, 0x530E}	{0x5310, 0x5311, 0x5312}	{0x5314, 0x5315, 0x5316}
short	{0x5340, 0x5341}	{0x5342, 0x5343}	{0x5344, 0x5345}	{0x5346, 0x5347}	{0x5348, 0x5349, 0x534A}	{0x534C, 0x534D, 0x534E}	{0x5350, 0x5351, 0x5352}	{0x5354, 0x5355, 0x5356}

table 5-3 MWB control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5000	R ISP CTRL00	0x9E	RW	Bit[1]: r_awbg_en AWB gain enable
0x5300	R GAIN B L	0x04	RW	B Gain in Long Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_b_l[13:8]
0x5301	R GAIN B L	0x00	RW	B Gain in Long Exposure Bit[7:0]: r_gain_b_l[7:0]
0x5302	R GAIN GB L	0x04	RW	Gb Gain in Long Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_gb_l[13:8]
0x5303	R GAIN GB L_L	0x00	RW	Gb Gain in Long Exposure Bit[7:0]: r_gain_gb_l[7:0]

table 5-3 MWB control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5304	R GAIN GR L_H	0x04	RW	Gr Gain in Long Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_gr_l[13:8]
0x5305	R GAIN GR L_L	0x00	RW	Gr Gain in Long Exposure Bit[7:0]: r_gain_gr_l[7:0]
0x5306	R GAIN R L_H	0x04	RW	R Gain in Long Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_r_l[13:8]
0x5307	R GAIN R L_L	0x00	RW	R Gain in Long Exposure Bit[7:0]: r_gain_r_l[7:0]
0x5308	R OFFSET B L_H	0x00	RW	B Offset in Long Exposure Bit[7:0]: r_offset_b_l[23:16]
0x5309	R OFFSET B L_M	0x00	RW	B Offset in Long Exposure Bit[7:0]: r_offset_b_l[15:8]
0x530A	R OFFSET B L_L	0x00	RW	B Offset in Long Exposure Bit[7:0]: r_offset_b_l[7:0]
0x530B	NOT USED	–	–	Not Used
0x530C	R OFFSET GB L_H	0x00	RW	Gb Offset in Long Exposure Bit[7:0]: r_offset_gb_l[23:16]
0x530D	R OFFSET GB L_M	0x00	RW	Gb Offset in Long Exposure Bit[7:0]: r_offset_gb_l[15:8]
0x5310	R OFFSET GR L_H	0x00	RW	Gr Offset in Long Exposure Bit[7:0]: r_offset_gr_l[23:16]
0x5311	R OFFSET GR L_M	0x00	RW	Gr Offset in Long Exposure Bit[7:0]: r_offset_gr_l[15:8]
0x5312	R OFFSET GR L_L	0x00	RW	Gr Offset in Long Exposure Bit[7:0]: r_offset_gr_l[7:0]
0x5314	R OFFSET R L_H	0x00	RW	R Offset in Long Exposure Bit[7:0]: r_offset_r_l[23:16]
0x5315	R OFFSET R L_M	0x00	RW	R Offset in Long Exposure Bit[7:0]: r_offset_r_l[15:8]
0x5316	R OFFSET R L_L	0x00	RW	R Offset in Long Exposure Bit[7:0]: r_offset_r_l[7:0]
0x5340	R GAIN B S_H	0x04	RW	B Gain in Short Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_b_s[13:8]
0x5341	R GAIN B S_L	0x00	RW	B Gain in Short Exposure Bit[7:0]: r_gain_b_s[7:0]

table 5-3 MWB control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5342	R GAIN GB S_H	0x04	RW	Gb Gain in Short Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_gb_s[13:8]
0x5343	R GAIN GB S_L	0x00	RW	Gb Gain in Short Exposure Bit[7:0]: r_gain_gb_s[7:0]
0x5344	R GAIN GR S_H	0x04	RW	Gr Gain in Short Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_gr_s[13:8]
0x5345	R GAIN GR S_L	0x00	RW	Gr Gain in Short Exposure Bit[7:0]: r_gain_gr_s[7:0]
0x5346	R GAIN R S_H	0x04	RW	R Gain in Short Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_r_s[13:8]
0x5347	R GAIN R S_L	0x00	RW	R Gain in Short Exposure Bit[7:0]: r_gain_r_s[7:0]
0x5348	R OFFSET B S_H	0x00	RW	B Offset in short Exposure Bit[7:0]: r_offset_b_s[23:16]
0x5349	R OFFSET B S_M	0x00	RW	B Offset in Short Exposure Bit[7:0]: r_offset_b_s[15:8]
0x534A	R OFFSET B S_L	0x00	RW	B Offset in Short Exposure Bit[7:0]: r_offset_b_s[7:0]
0x534C	R OFFSET GB S_H	0x00	RW	Gb Offset in Short Exposure Bit[7:0]: r_offset_gb_s[23:16]
0x534D	R OFFSET GB S_M	0x00	RW	Gb Offset in Short Exposure Bit[7:0]: r_offset_gb_s[15:8]
0x534E	R OFFSET GB S_L	0x00	RW	Gb Offset in Short Exposure Bit[7:0]: r_offset_gb_s[7:0]
0x5350	R OFFSET GR S_H	0x00	RW	Gr Offset in Short Exposure Bit[7:0]: r_offset_gr_s[23:16]
0x5351	R OFFSET GR S_M	0x00	RW	Gr Offset in Short Exposure Bit[7:0]: r_offset_gr_s[15:8]
0x5352	R OFFSET GR S_L	0x00	RW	Gr Offset in Short Exposure Bit[7:0]: r_offset_gr_s[7:0]
0x5354	R OFFSET R S_H	0x00	RW	R Offset in Short Exposure Bit[7:0]: r_offset_r_s[23:16]
0x5355	R OFFSET R S_M	0x00	RW	R Offset in Short Exposure Bit[7:0]: r_offset_r_s[15:8]

table 5-3 MWB control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5356	R OFFSET R S_L	0x00	RW	R Offset in Short Exposure Bit[7:0]: r_offset_r_s[7:0]
0x818C~ 0x818D	MAXIMUM B WB GAIN	–	RW	Maximum B WB Gain
0x818E~ 0x818F	MAXIMUM G WB GAIN	–	RW	Maximum G WB Gain
0x8190~ 0x8191	MAXIMUM R WB GAIN	–	RW	Maximum R WB Gain
0x81FC~ 0x81FD	LONG EXPOSURE MANUAL B WB GAIN	–	RW	Manual B WB Gain of Long Exposure
0x81FE~ 0x81FF	LONG EXPOSURE MANUAL GB WB GAIN	–	RW	Manual Gb WB Gain of Long Exposure
0x8200~ 0x8201	LONG EXPOSURE MANUAL GR WB GAIN	–	RW	Manual Gr WB Gain of Long Exposure
0x8202~ 0x8203	LONG EXPOSURE MANUAL R WB GAIN	–	RW	Manual R WB Gain of Long Exposure
0x820C~ 0x820D	SHORT EXPOSURE MANUAL B WB GAIN	–	RW	Manual B WB Gain of Short Exposure
0x820E~ 0x820F	SHORT EXPOSURE MANUAL GB WB GAIN	–	RW	Manual Gb WB Gain of Short Exposure
0x8210~ 0x8211	SHORT EXPOSURE MANUAL GR WB GAIN	–	RW	Manual Gr WB Gain of Short Exposure
0x8212~ 0x8213	SHORT EXPOSURE MANUAL R WB GAIN	–	RW	Manual R WB Gain of Short Exposure

5.7 PDC

The PDC receives location information (0x53xx) of the PD pixels in the array and removes them from the image. The PDC function supports PD compensation and PD correction.

The PD compensation function compensates for the intensity loss because of the PD mask. It is an essential step before PD correction. It is only applied to PD pixels. After compensation, the PD pixels' level is close to normal pixels. The PD compensation function can be turned on and off using register bit 0x5001[1]. The PDC compensation function compensates according to a ratio and fading list. The ratio and fading list is defined by registers 0x5D00~0x5D1B.

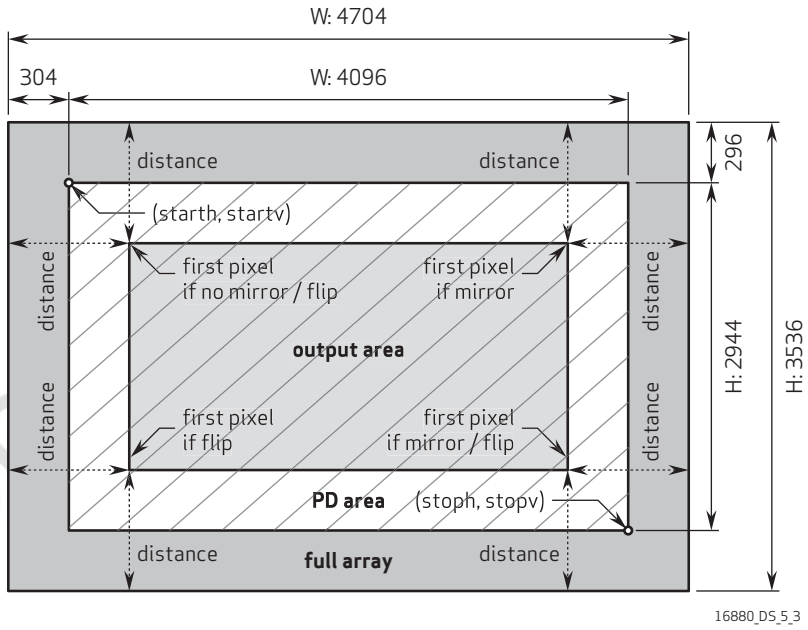
The PD correction function corrects PD pixels to normal pixels. The PD correction function can be turned on and off using register bit 0x5694[7]. To turn on the PD correction function, DPC must be turned on by setting register bit 0x5001[6] = 1.

PD pixels are evenly arranged in the PD area. All PD pixels are clear pixels in B channel.

PD pixel data can be read out. The area where PD pixel data can be read out is defined by registers 0x5D1C~0x5D23.

Registers 0x5D24~0x5D27 define the distance from the first pixel to the array edge that is received by PD compensation. The first pixel location changes when the output is mirrored or flipped (see **figure 5-3**).

figure 5-3 first pixel in PD area



To receive the correct location of the PD pixels, set the address of the PD pixels in the array using registers 0x5D2A~0x5D31. Registers {0x5D2C, 0x5D2D} (stoph) and {0x5D30, 0x5D31} (stopv) are the coordinates of the last pixels+1.

- registers 0x5D34~0x5D37 defines the full array size
- register 0x5D38: 2^19/(array width)
- register 0x5D39: 2^19/(array height)

In a 32x32 pattern PD compensation table, set the value of the bit to 1 if it is a PD pixel.

table 5-4 PDC registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x5500~ 0x557F	PDC MAP 00~31	–	–	PDC Map Registers
0x5D00~ 0x5D07	REVERSE RATIO 0~3	–	–	Reverse Ratio

table 5-4 PDC registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x5D08~ 0x5D1B	FADING LIST 0~4	–	–	Fading List
0x5D1C	FOCUS WIN LEFT	0x00	RW	Bit[4:0]: focus_win_left[12:8]
0x5D1D	FOCUS WIN LEFT	0x00	RW	Bit[7:0]: focus_win_left[7:0]
0x5D1E	FOCUS WIN TOP	0x00	RW	Bit[4:0]: focus_win_top[12:8]
0x5D1F	FOCUS WIN TOP	0x00	RW	Bit[7:0]: focus_win_top[7:0]
0x5D20	FOCUS WIN WIDTH	0x16	RW	Bit[4:0]: focus_win_width[12:8]
0x5D21	FOCUS WIN WIDTH	0x20	RW	Bit[7:0]: focus_win_width[7:0]
0x5D22	FOCUS WIN HEIGHT	0x10	RW	Bit[4:0]: focus_win_height[12:8]
0x5D23	FOCUS WIN HEIGHT	0xA0	RW	Bit[7:0]: focus_win_height[7:0]
0x5D24~ 0x5D44	PD CORRECTION CONTROL	–	–	PD Correction Control
0x567B~ 0x56A5	PD CORRECTION CONTROL	–	–	PD Correction Control
0x5D24	X OFFSET MAN	0x00	RW	Bit[4:0]: x_offset_man[12:8]
0x5D25	X OFFSET MAN	0x00	RW	Bit[7:0]: x_offset_man[7:0]
0x5D26	Y OFFSET MAN	0x00	RW	Bit[4:0]: y_offset_man[12:8]
0x5D27	Y OFFSET MAN	0x00	RW	Bit[7:0]: y_offset_man[7:0]
0x5D28	R PDC CTRL1 RW	0x80	RW	Bit[7]: blc_en Bit[6]: offset_man_en Bit[5]: y_bin_man_en Bit[4]: y_bin_man Bit[3]: mirror_man_enable Bit[2]: mirror_man Bit[1]: flip_man_enable Bit[0]: flip_man
0x5D29	R PDC CTRL2 RW	0x00	RW	Bit[7]: before_comp_en Bit[6]: focus_win_en Bit[5]: h_bin_man_en Bit[4]: h_bin_man Bit[3]: fix_ptn_en Bit[2]: fix_ptn_mode Bit[1]: h_bin4_en Bit[0]: v_bin4_en
0x5D2A	STARTH	0x02	RW	Bit[4:0]: Starth[12:8]
0x5D2B	STARTH	0xD0	RW	Bit[7:0]: Starth[7:0]
0x5D2C	STOPH	0x13	RW	Bit[4:0]: Stoph[12:8]

table 5-4 PDC registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x5D2D	STOPH	0x50	RW	Bit[7:0]: Stoph[7:0]
0x5D2E	STARTV	0x02	RW	Bit[4:0]: Startv[12:8]
0x5D2F	STARTV	0x20	RW	Bit[7:0]: Startv[7:0]
0x5D30	STOPV	0x0E	RW	Bit[4:0]: Stopv[12:8]
0x5D31	STOPV	0x80	RW	Bit[7:0]: Stopv[7:0]
0x5D32	R PDC CTRL3 RW	0x10	RW	Bit[6]: zone_man_en Bit[5]: bypass_ratio Bit[4]: rl_channel 3 Bit[3]: Ratio mirror manual enable Bit[2]: Ratio mirror manual Bit[1]: Ratio flip manual enable Bit[0]: Ratio flip manual
0x5D34	ARRAY W	0x16	RW	Bit[4:0]: array_w[12:8]
0x5D35	ARRAY W	0x20	RW	Bit[7:0]: array_w[7:0]
0x5D36	ARRAY H	0x10	RW	Bit[4:0]: array_h[12:8]
0x5D37	ARRAY H	0xA0	RW	Bit[7:0]: array_h[7:0]
0x5D38	FADING SCALERH	0x5D	RW	Bit[7:0]: fading_scalerh
0x5D39	FADING SCALERV	0x7C	RW	Bit[7:0]: fading_scalerv
0x5D40	X OFFSET	–	R	Bit[4:0]: x_offset[12:8]
0x5D41	X OFFSET	–	R	Bit[7:0]: x_offset[7:0]
0x5D42	Y OFFSET	–	R	Bit[4:0]: y_offset[12:8]
0x5D43	Y OFFSET	–	R	Bit[7:0]: y_offset[7:0]
0x5D44	R PDC CTRL R0	–	R	Bit[3]: h_bin_en Bit[2]: y_bin_en Bit[1]: Mirror Bit[0]: Flip

table 5-5 PDC correction registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5580~ 0x55FF	PDF MAP 00~31	–	–	PDF Map Registers
0x567B	R CTRL7B	0x00	RW	Bit[7]: ptn_man_en Bit[5:4]: man_expo_mode Bit[3:2]: man_cfa_ptn Bit[1:0]: man_hdr_ptn
0x567C	R CTRL7C	0x00	RW	Bit[7]: pd_ptn_man_en Bit[6]: zone_man_en Bit[5:4]: pd_man_expo_mode Bit[3:2]: pd_man_cfa_ptn Bit[1:0]: pd_man_hdr_ptn
0x5680	RO WTHRE	–	R	Bit[7:0]: ro_wthre[7:0]
0x5681	RO BTHRE	–	R	Bit[7:0]: ro_bthre[7:0]
0x5682	RO RATIO	–	R	Bit[3:0]: ro_ratio[3:0]
0x5683	RO LEVEL	–	R	Bit[1:0]: ro_level[1:0]
0x5684	X OFFSET	–	R	Bit[4:0]: x_offset[12:8]
0x5685	X OFFSET	–	R	Bit[7:0]: x_offset[7:0]
0x5686	Y OFFSET	–	R	Bit[4:0]: y_offset[12:8]
0x5687	Y OFFSET	–	R	Bit[7:0]: y_offset[7:0]
0x5688	R PDF CTRL RO	–	R	Bit[3]: h_bin_en Bit[2]: v_bin_en Bit[1]: Mirror Bit[0]: Flip
0x5690	X OFFSET MAN	0x00	RW	Bit[4:0]: x_offset_man[12:8]
0x5691	X OFFSET MAN	0x00	RW	Bit[7:0]: x_offset_man[7:0]
0x5692	Y OFFSET MAN	0x00	RW	Bit[3:0]: y_offset_man[11:8]
0x5693	Y OFFSET MAN	0x00	RW	Bit[7:0]: y_offset_man[7:0]
0x5694	R PDF CTRL1	0x00	RW	Bit[7]: pd_remove_en Bit[6]: offset_man_en Bit[5]: v_bin_man_en Bit[4]: v_bin_man Bit[3]: mirror_man_en Bit[2]: mirror_man Bit[1]: flip_man_en Bit[0]: flip_man

table 5-5 PDC correction registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5695	R PDF CTRL2	0x00	RW	Bit[7:6]: flag_dly_num Bit[5]: h_bin_man_en Bit[4]: h_bin_man Bit[3]: fix_ptn_en Bit[2]: fix_ptn_mode Bit[1:0]: Not used
0x5696	WEIGHT C	0x08	RW	Bit[4:0]: weight_c[4:0]
0x5697	WEIGHT D	0x08	RW	Bit[4:0]: weight_d[4:0]
0x5698	STARTH	0x02	RW	Bit[4:0]: Starth[12:8]
0x5699	STARTH	0xD0	RW	Bit[7:0]: Starth[7:0]
0x569A	STOPH	0x13	RW	Bit[4:0]: Stoph[12:8]
0x569B	STOPH	0x50	RW	Bit[7:0]: Stoph[7:0]
0x569C	STARTV	0x02	RW	Bit[4:0]: Startv[12:8]
0x569D	STARTV	0x20	RW	Bit[7:0]: Startv[7:0]
0x569E	STOPV	0x0E	RW	Bit[4:0]: Stopv[12:8]
0x569F	STOPV	0x80	RW	Bit[7:0]: Stopv[7:0]
0x56A0	R PDF CTRL5	0x36	RW	Bit[7]: dis_d2_to_d4 Bit[6]: odd_green_rvs Bit[5]: rl_channel3 Bit[4]: ext_en Bit[3:2]: ext_ptn3 Bit[1:0]: ext_ptn4
0x56A1	SHADOW TH	0x40	RW	Bit[6:0]: shadow_th[6:0]
0x56A2	ARRAY W	0x16	RW	Bit[4:0]: array_w[12:8]
0x56A3	ARRAY W	0x20	RW	Bit[7:0]: array_w[7:0]
0x56A4	ARRAY H	0x10	RW	Bit[4:0]: array_h[12:8]
0x56A5	ARRAY H	0xA0	RW	Bit[7:0]: array_h[7:0]

5.8 window

ISP output window module's input data is 16 bit-width. The window module can crop the output picture by any size. The output size can be both automatically generated or manually set by register bit 0x5C08[0]. In manual mode, registers {0x5C00, 0x5C01} are used to define horizontal start point and registers {0x5C02, 0x5c03} are used to define vertical start point. Registers {0x5C04, 0x5C05} and {0x5C06, 0x5C07} are used to define width and height of the output picture.

6 register tables

The following tables provide descriptions of the device control registers contained in the OV16880. For all registers enable/disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 0x6C for write and 0x6D for read when SID=0 (when SID=1, 0x20 for write and 0x21 for read).

6.1 sleep/sw_reset control

table 6-1 sleep/sw_reset control registers

address	register name	default value	R/W	description
0x0100	CTRL00	0x00	RW	Bit[0]: Software standby 1: Streaming
0x0102	CTRL01	0x00	RW	Bit[0]: Truncation standby mode
0x0103	CTRL02	–	W	Bit[0]: software_reset

6.2 PLL control [0x0300 - 0x0313, 0x031B - 0x031C, 0x031E]

table 6-2 PLL control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x0100	CTRL00	0x00	RW	Bit[0]: Software standby 1: Streaming
0x0102	CTRL01	0x00	RW	Bit[0]: Truncation standby mode
0x0103	CTRL02	–	W	Bit[0]: software_reset
0x0300	PLL1 PRE DIV	0x00	RW	Bit[7:3]: Not used Bit[2:0]: PLL1 pre_div 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x0301	PLL1 MULTI1	0x00	RW	Bit[7:2]: Not used Bit[2:0]: pll1_multi[9:8]
0x0302	PLL1 MULTI0	0x3C	RW	Bit[7:0]: PLL1 multiplier[7:0]

table 6-2 PLL control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x0303	PLL1 DIV M	0x00	RW	Bit[7:4]: Not used Bit[3:0]: PLL1 divm 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16
0x0304	PLL1 DIV MIPI	0x07	RW	Bit[7:3]: Not used Bit[2:0]: PLL1 div_mipi 000: /4 001: /5 010: /6 011: /7 100: /8 Others: /8
0x0305	PLL1 DIV SP	0x01	RW	Bit[7:2]: Not used Bit[1:0]: PLL1 div_sp 00: /3 01: /4 10: /5 11: /6
0x0306	PLL1 DIV S	0x01	RW	Bit[7:1]: Not used Bit[0]: PLL1 div_s 0: /1 1: /2
0x0307	RSVD	–	–	Reserved
0x0308	PLL1 BYP	0x00	RW	Bit[7:1]: Not used Bit[0]: PLL1 bypass
0x0309	PLL1 CP	0x01	RW	Bit[7:3]: Not used Bit[2:0]: pll1_cp

table 6-2 PLL control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x030A	PLL1 CTR	0x00	RW	Bit[7:2]: Not used Bit[1]: pll1_div_rst_sync_en Bit[0]: pll1_predivp 0: /1 1: /2
0x030B	PLL2 PRE DIV	0x00	RW	Bit[7:3]: Not used Bit[2:0]: pll2_pre_div 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /4 110: /6 111: /8
0x030C	PLL2 DIVP1	0x00	RW	Bit[7:2]: Not used Bit[1:0]: PLL2 divp[9:8]
0x030D	PLL2 DIVP0	0x28	RW	Bit[7:0]: PLL2 divp[7:0]
0x030E	PLL2 DIVS	0x02	RW	Bit[7:3]: Not used Bit[2:0]: pll2_divs 000: /1 001: /1.5 010: /2 011: /2.5 100: /3 101: /3.5 110: /4 111: /5
0x030F	PLL2 DIVSP	0x03	RW	Bit[7:4]: Not used Bit[3:0]: pll2_divsp 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16

table 6-2 PLL control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x0310	PLL2 CP	0x01	RW	Bit[7:3]: Not used Bit[2:0]: pll2_cp
0x0311	PLL2 PREDIVP	0x00	RW	Bit[7:1]: Not used Bit[0]: pll2_predivp 0: /1 1: /2
0x0312	PLL CTR0	0x03	RW	Bit[7:5]: Not used Bit[4]: PLL2 bypass Bit[3:0]: pll2_divdac 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16
0x0313	PLL2 CTR1	0x00	RW	Bit[7:5]: Not used Bit[4]: pll2_div_rst_sync_en Bit[3:0]: pll2_div_sram 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16
0x031B	PLL1 RST	0x00	RW	Bit[0]: pll1_rst_o
0x031C	PLL2 RST	0x00	RW	Bit[0]: pll2_rst_o

table 6-2 PLL control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x031E	CTRL1E	0x09	RW	Bit[7:4]: Not used Bit[3]: PLL1 no lat Bit[2:0]: mipi_bit mode 00: 8-bit 01: 10-bit 10: 12-bit 11: Not used

6.3 system control [0x3000 - 0x302A, 0x302C, 0x3031 - 0x303F, 0x3660 - 0x3673]

table 6-3 system control registers (sheet 1 of 9)

address	register name	default value	R/W	description
0x3000	IO PAD OEN	0x00	RW	Input/Output Control (0: input, 1: output) Bit[7:2]: Not used Bit[1:0]: Reserved
0x3001	IO PAD OEN	0x03	RW	Input/Output Control (0: input, 1: output) Bit[7:3]: Reserved Bit[2]: gpio4_oen Bit[1]: gpio3_oen when AFC SCCB disable Bit[0]: gpio2_oen
0x3002	IO PAD OEN	0x00	RW	Bit[7]: io_vsync_oen Bit[6]: io_href_oen Bit[5]: Reserved Bit[4]: io_frex_oen Bit[3]: io_fsin_oen Bit[2]: Reserved Bit[1]: io_gpio1_oen Bit[0]: io_gpio0_oen
0x3003	IO PAD OUT	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Reserved
0x3004	IO PAD OUT	0x04	RW	Output Value Bit[7:3]: Not used Bit[2]: io_gpio4_o Bit[1]: io_gpio3_o Bit[0]: io_gpio2_o

table 6-3 system control registers (sheet 2 of 9)

address	register name	default value	R/W	description
0x3005	IO PAD OUT	0x00	RW	Bit[7]: io_vsync_o Bit[6]: io_href_o Bit[5]: io_il_pwm Bit[4]: io_frex_o Bit[3]: io_fsin_o Bit[2]: io_strobe_o Bit[1]: io_gpio1_o Bit[0]: io_gpio0_o
0x3006	IO PAD SEL	0x00	RW	Bit[7:2]: Not used Bit[1:0]: Reserved
0x3007	IO PAD SEL	0x04	RW	Output Selection (0: normal data path, 1: register control value) Bit[7:3] Reserved Bit[2]: ip_gpio4_sel Bit[1]: ip_gpio3_sel Bit[0]: ip_gpio2_sel
0x3008	PAD SEL2	0x00	RW	Output Selection (0: normal data path, 1: register control value) Bit[7]: io_vsync_sel Bit[6]: io_href_sel Bit[5]: io_frex_sel Bit[4]: io_strobe_sel Bit[3]: io_fsin_sel Bit[2]: io_il_pwm_sel Bit[1]: io_gpio1_sel Bit[0]: io_gpio0_sel
0x3009	PAD CTRL	0x06	RW	Bit[7:0]: a_pad_pk_o
0x300A	CHIP ID BK	0x01	R	Bit[7:0]: chip_id_bk[23:16]
0x300B	CHIP ID BK	0x68	R	Bit[7:0]: chip_id_bk[15:8]
0x300C	CHIP ID BK	0x80	R	Bit[7:0]: chip_id_bk[7:0]
0x300D	PUMP CLK CTRL	0x15	RW	Bit[7]: Not used Bit[6:4]: p_pump_clk_div Bit[3]: Reserved Bit[2:0]: n_pump_clk_div
0x300E	DUMMY	0x00	RW	Bit[7:0]: Not used
0x300F	MIPI SC	0x11	RW	Bit[7]: mipi_cphy_dis2 Bit[6]: mipi_cphy_dis1 Bit[5]: mipi_cphy_dis0 Bit[4]: mipi_en Bit[3:2]: Reserved Bit[1:0]: mipi_bit_sel_o
0x3010	MIPI PK	0x00	RW	Bit[7:0]: a_mipi_pk_o[15:8]

table 6-3 system control registers (sheet 3 of 9)

address	register name	default value	R/W	description
0x3011	MIPI PK	0x04	RW	Bit[7:0]: a_mipi_pk_o[7:0]
0x3012	MIPI SC CTRL0	0x41	RW	Bt[7:6]: lane_num 00: 0 lane 01: 1 lane 10: 2 lane 11: 4 lane Bit[3]: Reserved Bit[2]: r_phy_pd_mipi manual 1: Power down PHY HS TX Bit[1]: mipi_ck_lp_dir Bit[0]: phy_pad_en
0x3013	MIPI SC CTRL1	0x00	RW	Bit[7:6]: mipi_d4_skew Bit[5:4]: mipi_d3_skew Bit[3:2]: mipi_d2_skew Bit[1:0]: mipi_d1_skew
0x3014	MIPI SC CTRL2	0x00	RW	Bit[7:0]: Not used
0x3015	MIPI SC CTRL3	0x00	RW	Bit[7]: mipi_lane_dis4 Bit[6]: mipi_lane_dis3 Bit[5]: mipi_lane_dis2 Bit[4]: mipi_lane_dis1 Bit[3]: mipi_ck_lane_dis Bit[2]: Reserved Bit[1:0]: mipi_ck0_skew_o
0x3016	CLKRST0	0xF0	RW	Bit[7]: sclk_ac Bit[6]: sclk_stb Bit[5]: sclk_pdfifo Bit[4]: sclk_tc Bit[3]: rst_ac Bit[2]: rst_stb Bit[1]: rst_pdfifo Bit[0]: rst_tc
0x3017	CLKRST1	0xF0	RW	Bit[7]: sclk_tpm Bit[6]: sclk_isp Bit[5]: sclk_arb Bit[4]: sclk_vfifo Bit[3]: rst_tpm Bit[2]: rst_isp Bit[1]: rst_arb Bit[0]: rst_vfifo

table 6-3 system control registers (sheet 4 of 9)

address	register name	default value	R/W	description
0x3018	CLKRST2	0xF0	RW	Bit[7]: pclk_pdfifo Bit[6]: sclk_mipi Bit[5]: sclk_hsub Bit[4]: sclk_otp Bit[3]: rst_lvds Bit[2]: rst_mipi Bit[1]: rst_hsub Bit[0]: rst_otp
0x3019	CLKRST3	0xF0	RW	Bit[7]: sclk_blc Bit[6]: sclk_ispfc Bit[5]: sclk_fmt Bit[4]: sclk_embline Bit[3]: rst_blc Bit[2]: rst_ispfc Bit[1]: rst_fmt Bit[0]: rst_embline
0x301A	CLKRST4	0xF0	RW	Bit[7]: sclk_grp Bit[6]: padclk_mipi_sc Bit[5]: pclk_vfifo Bit[4]: pclk_mipi Bit[3]: rst_grp Bit[2]: rst_mipi_sc Bit[1]: rst_illum Bit[0]: rst_emline manual
0x301B	CLKRST5	0xB4	RW	Bit[7:6]: dac_clk_sel Bit[5]: sclk_bist20 Bit[4]: sclk_snr_sync Bit[3]: sclk_grp_fix Bit[2]: dacclk_en Bit[1]: rst_bist20 Bit[0]: rst_snr_sync
0x301C	FREX RST MASK0	0x01	RW	Bit[7]: frex_mask_dpcm Bit[6]: frex_mask_illum Bit[5]: frex_mask_sync_fifo Bit[4]: frex_mask_emb Bit[3]: frex_mask_ispfc Bit[2]: frex_mask_blc Bit[1]: frex_mask_hsub Bit[0]: frex_mask_stb
0x301D	FREX RST MASK0	0x02	RW	Bit[7]: frex_mask_pdfifo Bit[6]: frex_mask_tpm Bit[5]: frex_mask_isp Bit[4]: frex_mask_lvds Bit[3]: frex_mask_mipi Bit[2]: frex_mask_fmt Bit[1]: frex_mask_arb Bit[0]: frex_mask_mipi_phy

table 6-3 system control registers (sheet 5 of 9)

address	register name	default value	R/W	description
0x301E	CLOCK SEL	0x10	RW	Bit[7:6]: Reserved Bit[5]: clk_sw_pll Bit[4]: clk_sw_pad Bit[3]: pclk_div 0: /1 1: /2 Bit[2:1]: sclk_sel 0: /1 1: /2 Bit[0]: sclk2x_sel
0x301F	MISC CTRL	0x03	RW	Bit[7:1]: Not used Bit[0]: cen_global_o
0x3020	LOW PWR CTR	0x00	RW	Bit[7]: Not used Bit[6]: phy_pd_mipi_pwdn_dis Bit[5]: Reserved Bit[4]: stb_rst_dis 0: Reset all blocks at software standby mode 1: Tc, sensor_control, ISP are reset, others not Bit[3:2]: Reserved Bit[1]: phy_pd_mipi_slppd_dis Bit[0]: Reserved
0x3021	A PWC PK O	0x00	RW	Bit[7:0]: a_pwc_pk_o
0x3022	CLKRST6	0x0F	RW	Bit[7]: sclk_ba22 Bit[6]: sclk_rom Bit[5]: sclk_uart Bit[4]: sclk_sram Bit[3]: rst_ba22 Bit[2]: rst_rom Bit[1]: rst_sram Bit[0]: rst_uart
0x3023	CLKRST7	0xF0	RW	Bit[7]: sclk_psv Bit[6]: sclk_mipirx Bit[5]: sclk_fc Bit[4]: sclk_sccb Bit[3]: rst_psv Bit[2]: rst_mipirx Bit[1]: rst_fc Bit[0]: Not used

table 6-3 system control registers (sheet 6 of 9)

address	register name	default value	R/W	description
0x3024	FREX RST MASK	0xF0	RW	Bit[7]: frex_mask_ba22 Bit[6]: frex_mask_rom Bit[5]: frex_mask_sram Bit[4]: frex_mask_uart Bit[3]: frex_mask_fc Bit[2]: frex_mask_mipirx Bit[1:0]: Not used
0x3025	PSV MODE OPT	0x02	RW	Bit[7]: npump_clk_ausw_dis Bit[6]: pump_clk_sw Bit[5]: ppump_clk_ausw_dis Bit[4]: daclk_cutoff_byp Bit[3]: sclk2x_cutoff_byp Bit[2]: pclk_cutoff_byp Bit[1]: clk_cutoff_byp Bit[0]: auto_sleep_en
0x3026	CLK GATE MASK	0x00	RW	Bit[7]: sclk_dpcm Bit[6]: sclk_blc_cali_mini Bit[5]: sclk_blc_cali Bit[4]: pclk_mipi Bit[3]: pclk_vfifo Bit[2]: pclk_pdfifo Bit[1]: sclk_snr_sync Bit[0]: sclk_emb
0x3027	CLK GATE MASK	0x00	RW	Bit[7]: sclk_fmt Bit[6]: sclk_ispfc Bit[5]: sclk_blc Bit[4]: sclk_hsub Bit[3]: sclk_mipi Bit[2]: sclk_vfifo Bit[1]: sclk_isp Bit[0]: sclk_pdfifo
0x3028	CTRL28	0xB4	RW	Bit[7]: Not used Bit[6]: sclk_dpcm Bit[5]: sclk_blc_cali_mini Bit[4]: sclk_blc_cali Bit[3]: Not used Bit[2]: rst_dpcm Bit[1]: rst_blc_cali_mini Bit[0]: rst_blc_cali
0x3029	FREX_MASK_BLC_CALI_MINI	0x00	RW	Bit[7:2]: Not used Bit[1]: frex_mask_blc_cali_mini Bit[0]: frex_mask_blc_cali
0x302A	CHIP REVISION	0xB0	RW	Bit[7:0]: chip_revision
0x302C	RSVD	–	–	Reserved

table 6-3 system control registers (sheet 7 of 9)

address	register name	default value	R/W	description
0x3031	MIPI PK	0x91	RW	Bit[7]: Not used Bit[6:0]: a_mipi_pk_o[22:16]
0x3032~ 0x3033	RSVD	–	–	Reserved
0x3034	MIPI2 CTRL4	0x41	RW	Bit[7:0]: Reserved
0x3035	SC_SCCB_ID	0x6C	RW	Bit[7:0]: SCCB ID
0x3036	SC_SCCB_ID	0x42	RW	Bit[7:0]: SCCB ID2
0x3037	SC_SCCB_ID	0x20	RW	Bit[7:0]: SCCB alternate ID
0x3038	SC_SCCB_ID	0x00	RW	Bit[7:0]: SCCB ID2 NACK
0x3039	MIPI2 CTRL0	0x11	RW	Bit[7:0]: Reserved
0x303A	MIPI2 CTRL1	0x00	RW	Bit[7:0]: Reserved
0x303B	MIPI2 CTRL2	0x00	RW	Bit[7:0]: Reserved
0x303C	MIPI2 CTRL3	0x00	RW	Bit[7:0]: Reserved
0x303D	GP IO IN0	–	R	Bit[7:5]: Not used Bit[4]: tpm_db Bit[3:2]: slit_id Bit[3:0]: p_gpio[4:3]
0x303E	GP IO IN1	–	R	Bit[7:5]: p_gpio[2:0] Bit[4]: p_vsync_i Bit[3]: p_href_i Bit[2:0]: Reserved
0x303F	GP IO IN2	–	R	Bit[7:0]: Not used
0x3660	CORE 0	0xC0	RW	Bit[7]: rip_sof_en Bit[6]: rip_eof_en Bit[5]: MIPI 8-lane enable Bit[4]: r_blc_cali_tst Bit[3]: dpcm_bypass_in2 Bit[2]: dpcm_en (10~8-bit) Bit[1]: dpcm_en (12~10-bit) Bit[0]: y_rgbw_buf

table 6-3 system control registers (sheet 8 of 9)

address	register name	default value	R/W	description
0x3661	CORE 1	0x04	RW	Bit[7]: rst_mipi Bit[6]: rst_otp Bit[5]: rst_tpm Bit[4]: afc_mipi_align_en Bit[3]: afc_state_en Bit[2]: r_afc_data_en Bit[1]: PDAF control 0: PD data type mode enable 1: PD virtual channel mode enable Bit[0]: PDAF MIPI timing align enable
0x3662	CORE 2	0x00	RW	Bit[7:4]: hsub_ctrl0 Bit[3]: snr_data_clip_dis Bit[2:0]: snr_data_shift
0x3663	CORE 3	0x20	RW	Bit[7]: r_cen_global_sel Bit[6]: r_uart_out_en Bit[5]: Not used Bit[4]: r_pad_share_shutter_o_opt Bit[3:2]: r_pad_share_frex_o_opt Bit[1:0]: r_pad_share_strobe_o_opt
0x3664	CORE 4	0x08	RW	Bit[7]: r_pll2_sclk_sel Bit[6:4]: r_agc_high_gain_man Bit[3]: r_pll2_daclk_sel Bit[2]: lvds_vsync_sel Bit[1]: lvds_ck_data_sel Bit[0]: r_one_chn_blc_en
0x3665	CORE 5	0x12	RW	Bit[7]: emb_en Bit[6]: emb_data_lsb Bit[5:0]: r_emb_data_type
0x3666	CORE 6	0xA4	RW	Bit[7]: r_ispin_sw_auto Bit[6:5]: r_isp_in_sw Bit[4:0]: r_eof_dly
0x3667	CORE 7	0x00	RW	Bit[7]: AFC data type mode enable Bit[6]: pdfifo2_en Bit[5:0]: AFC data type value
0x3668	CORE 8	0x20	RW	Reserved
0x3669	CORE 9	0x00	RW	Bit[7]: r_pd_ramp Bit[6]: r_pd_clk_diff Bit[5]: r_pd_asram Bit[4]: r_pd_sa1 Bit[3]: r_mipi_pclk_sel Bit[2:0]: Not used

table 6-3 system control registers (sheet 9 of 9)

address	register name	default value	R/W	description
0x366A	CORE A	0x54	RW	Bit[7]: r_vfpn_byp Bit[6]: r_bshrt_vfpn_sw Bit[5]: r_blen_vfpn_sw Bit[4]: r_blsw_vfpn_sw Bit[3]: small_gain_lat_en Bit[2]: r_bshrt_vfpn Bit[1]: r_blen_vfpn Bit[0]: r_blsw_vfpn
0x366B	2X4 LANE MIPI CONTROL	0x00	RW	Half_line_overlap_pixel_number/4
0x366C	2X4 LANE MIPI CONTROL	0x00	RW	Bit[7]: r_pcxsa_auto_dis Bit[6]: r_afc_done_out_en Bit[5]: r_pd_data_rev Bit[4]: r_pd_data_en Bit[3]: r_pd_low8 Bit[2]: r_mipi_2x4_md3_align Bit[1:0]: MIPI 2x4 line mode 00: Function disable 01: Even-odd pixel mode 10: 4 pixel mode 11: Half row mode
0x366D	CORE D	0x88	RW	Bit[7:4]: r_vref_bit_clamp_2x Bit[3:0]: r_vref_bit_clamp_1x
0x366E	CORE E	0x88	RW	Bit[7:4]: r_vref_bit_clamp_8x Bit[3:0]: r_vref_bit_clamp_4x
0x366F	CORE F	0x77	RW	Bit[7:4]: r_vrfd_4x Bit[3:0]: r_vrfd_2x
0x3670	CORE 10	0x07	RW	Bit[3:0]: r_vrfd_8x
0x3671	CORE 11	0x00	RW	Bit[7:0]: r_pwc_pk_2x
0x3672	CORE 12	0x00	RW	Bit[7:0]: r_pwc_pk_4x
0x3673	CORE 13	0x00	RW	Bit[7:0]: r_pwc_pk_8x

6.4 SCCB control [0xFFF0 - 0xFFFC]

table 6-4 SCCB control registers

address	register name	default value	R/W	description
0xFFF0~ 0xFFFC	DEBUG MODE	–	–	Debug Mode

6.5 group hold [0x3200 - 0x320F]

table 6-5 group hold registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3200	GROUP ADR0	0x00	RW	Group0 Start Address in SRAM Actual Address is {0x3200[5:0], 4'h0}
0x3201	GROUP ADR1	0x10	RW	Group1 Start Address in SRAM Actual Address is {0x3201[5:0], 4'h0}
0x3202	GROUP ADR2	0x20	RW	Group2 Start Address in SRAM Actual Address is {0x3202[5:0], 4'h0}
0x3203	GROUP ADR3	0x30	RW	Group3 Start Address in SRAM Actual Address is {0x3203[5:0], 4'h0}
0x3204	GROUP LEN0	–	R	Length of Group0
0x3205	GROUP LEN1	–	R	Length of Group1
0x3206	GROUP LEN2	–	R	Length of Group2
0x3207	GROUP LEN3	–	R	Length of Group3
0x3208	GROUP ACCESS	–	W	Group Access Bit[7:4]: group_ctrl 0000: Group hold start 0001: Group hold end 1010: Group delay launch 1110: Group quick launch Others: Debug mode Bit[3:0]: Group ID 0000: Group bank 0, default start from address 0x00 0001: Group bank 1, default start from address 0x40 0010: Group bank 2, default start from address 0x80 0011: Group bank 3, default start from address 0xB0 Others: Debug mode
0x3209	GROUP0 PERIOD	0x00	RW	Bit[7]: Not used Bit[6:5]: Switch back group In context switch, it must be group 0 Bit[4:0]: Number of frames to stay in first group

table 6-5 group hold registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x320A	GROUP1 PERIOD	0x00	RW	Number of Frames to Stay in Second Group
0x320B	GRP_SWCTRL	0x01	RW	Bit[7]: Auto switch Bit[6:4]: Not used Bit[3]: group_switch_repeat_en Enable the first group (group 0) and second group repeatable switch Bit[2]: context_en Enable to switch from second group back to first group (group 0) automatically Bit[1:0]: Second group selection
0x320C	SRAM TEST	0x0A	RW	Bit[7:5]: Not used Bit[4]: Group hold SRAM test enable Bit[3:0]: Group hold SRAM RM[3:0]
0x320D	GRP_ACT	–	R	Active Group Indicator
0x320E	FM_CNT_GRP0	–	R	Group 0 Frame Count
0x320F	FM_CNT_GRP1	–	R	Group 1 Frame Count

6.6 AFC control [0x3769 - 0x377F]

table 6-6 AFC control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3769	REG69	0x34	RW	Bit[7:4]: ptx_gap Bit[3:0]: ptx_start
0x376A	REG6A	0x0B	RW	Bit[7:0]: SRS end
0x376B	REG6B	0x83	RW	Bit[7:6]: Not used Bit[5]: sh_ldo_re Bit[4]: sh_ldo_al Bit[3:0]: sh_ldo_end
0x376C	REG6C	0x10	RW	Bit[7]: sr_pump_rst Bit[6]: sdivrst_f Bit[5]: Not used Bit[4]: smini_addr_man_en Bit[3]: smini_addr_bin4 Bit[2]: smini_addr_bin2 Bit[1:0]: smini_addr_man

table 6-6 AFC control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x376D	REG6D	0x01	RW	Bit[7:0]: sr_cnt_limit_h
0x376E	REG6E	0x80	RW	Bit[7:0]: sr_cnt_limit_l Total codes should x4, (dacclk is div2 in digital, counter use dual edge)
0x376F	REG6F	0x01	RW	Bit[7]: r_frex_addr_lat_opt Option for FREX mode Latch SP and RP address Bit[6]: r_no2p2_hdr4_en Option in HDR4 mode No padd2 and ppadd2 for 2 short exposure precharge Short exposure change cannot be larger than vblanking. Bit[5]: r_nopchg_rp_addr_en No precharge address on RP XADD bus Bit[4]: r_shrtexp_add_ppchg Option in HDR4 mode Add ppchg to e2 when e1 ppchg Add ppchg to e3 when e4 ppchg Always ppcharge short at long exposure Bit[3]: r_hdr_vflg_sw HDR mode vertical line flag switch Bit[2]: r_hdr_hflg_sw HDR mode horizontal line (half-line) flag switch Bit[1]: Flip HDR option Bit[0]: r_flip_opt Zadd counter option Pchg all zero lines
0x3770	REG70	0x00	RW	Bit[7:0]: r_af_addintv[15:8] AF frame vertical timing size high byte when auto size is disabled (works only when 0x379F[2] = 0)
0x3771	REG71	0x00	RW	Bit[7:0]: r_af_addintv[7:0] AF frame vertical timing size low byte when auto size is disabled (works only when 0x379F[2] = 0)

table 6-6 AFC control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3772	REG72	0x00	RW	Bit[7:0]: r_af_addbase[15:8] Vertical position at image frame, the first AF frame start from (works only when 0x379F[1] = 0)
0x3773	REG73	0x00	RW	Bit[7:0]: r_af_addbase[7:0] Vertical position at image frame, the first AF frame start from (works only when 0x379F[1] = 0)
0x3774	REG74	0x40	RW	Bit[7:0]: r_afc_line_num[7:0] Line number in one AF frame
0x3775	REG75	0x81	RW	Bit[7:6]: Not used Bit[5]: afc_extraln_opt Bit[4]: r_afc_line_num[8] Bit[3:0]: r_afc_grp enable
0x3776	REG76	0x31	RW	Bit[7:4]: r_afc_odd_inc AF line position interval at odd line Bit[3:0]: r_afc_even_inc AF line position interval at even line
0x3777	REG77	0x06	RW	Bit[7:0]: r_afc_start_addr0[15:8]
0x3778	REG78	0xA0	RW	Bit[7:0]: r_afc_start_addr0[7:0]
0x3779	REG79	0x00	RW	Bit[7:0]: r_afc_start_addr1[15:8]
0x377A	REG7A	0x00	RW	Bit[7:0]: r_afc_start_addr1[7:0]
0x377B	REG7B	0x00	RW	Bit[7:0]: r_afc_start_addr2[15:8]
0x377C	REG7C	0x00	RW	Bit[7:0]: r_afc_start_addr2[7:0]
0x377D	REG7D	0x00	RW	Bit[7:0]: r_afc_start_addr3[15:8]
0x377E	REG7E	0x00	RW	Bit[7:0]: r_afc_start_addr3[7:0]
0x377F	REG7F	0x31	RW	Bit[7:4]: r_afc_band_odd_inc AF line timing interval at odd line when output Bit[3:0]: r_afc_band_even_inc AF line timing interval at even line when output

6.7 AFC buffer [0x4B01 - 0x4B03, 0x4B05 - 0x4B0B, 0x4B10]

table 6-7 AFC buffer registers

address	register name	default value	R/W	description
0x4B01	R1	0x01	RW	Bit[7]: SCCB master enable Bit[6]: AFC_SCCB_master_hold_delay[2] Bit[5]: r_sram0_test Bit[4]: r_sram0_RME Bit[3:0]: r_sram0_RM
0x4B02	R2	0x01	RW	Bit[7]: r_recovery_dis Bit[6]: r_sram_wemb_sel Bit[5]: r_sram1_test Bit[4]: r_sram1_RME Bit[3:0]: r_sram1_RM
0x4B03	R3	0x06	RW	Bit[7]: SCCB master GPIO enable Bit[6]: NACK retry Bit[5]: r_sram2_test Bit[4]: r_sram2_RME Bit[3:0]: r_sram2_RM
0x4B05	R5	0x92	RW	Bit[7]: r_afc_bitclamp Bit[6:4]: r_afc_bitshft Bit[2]: r_no_eof Bit[1]: r_vc_split Bit[0]: r_byp
0x4B06	R6	0x00	RW	Bit[7]: afc_hskip4 Bit[6]: afc_hskip2 Bit[5]: afc_win_en Bit[4]: afc_win Manual set window offset enable Bit[2:0]: afc_win manual offset[10:8]
0x4B07	R7	0x00	RW	Bit[7:0]: afc_win manual offset[7:0]
0x4B08	R8	0x96	RW	Bit[7:0]: afc_sccb_speed AFC SCCB SCL period = 0x4B08 x 4 x Tsclk
0x4B09	R9	0xC0	RW	Bit[7:6]: AFC_SCCB_master_hold_delay[1:0] Bit[5:0]: afc_byte_num
0x4B0A	RA	0x00	RW	Bit[7:0]: afc_win_start[15:8]
0x4B0B	RB	0x08	RW	Bit[7:0]: afc_win_start[7:0]
0x4B10	R10	–	W	Bit[7:0]: afc_sccb_start Trigger AFC SCCB master to send data

6.8 timing control [0x3800 - 0x3849, 0x3850 - 0x3858, 0x3860 - 0x3863]

table 6-8 timing control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x3800	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[15:8] Array horizontal start point
0x3801	X ADDR START	0x00	RW	Bit[7:0]: x_addr_start[7:0] Array horizontal start point
0x3802	Y ADDR START	0x00	RW	Bit[7:0]: y_addr_start[15:8] Array vertical start point
0x3803	Y ADDR START	0x08	RW	Bit[7:0]: y_addr_start[7:0] Array vertical start point
0x3804	X ADDR END	0x12	RW	Bit[7:0]: x_addr_end[15:8] Array horizontal end point
0x3805	X ADDR END	0x5F	RW	Bit[7:0]: x_addr_end[7:0] Array horizontal end point
0x3806	Y ADDR END	0x0D	RW	Bit[7:0]: y_addr_end[15:8] Array vertical end point
0x3807	Y ADDR END	0xC7	RW	Bit[7:0]: y_addr_end[7:0] Array vertical end point
0x3808	X OUTPUT SIZE	0x12	RW	Bit[7:0]: x_output_size[15:8] ISP horizontal output width
0x3809	X OUTPUT SIZE	0x40	RW	Bit[7:0]: x_output_size[7:0] ISP horizontal output width
0x380A	Y OUTPUT SIZE	0x0D	RW	Bit[7:0]: y_output_size[15:8] ISP vertical output height
0x380B	Y OUTPUT SIZE	0xB0	RW	Bit[7:0]: y_output_size[7:0] ISP vertical output height
0x380C	TIMING_HTS	0x13	RW	Bit[7:0]: Horizontal total size[15:8]
0x380D	TIMING_HTS	0xA0	RW	Bit[7:0]: Horizontal total size[7:0]
0x380E	TIMING_VTS	0x0E	RW	Bit[7]: Not used Bit[6:0]: Vertical total size[14:8]
0x380F	TIMING_VTS	0xF0	RW	Bit[7:0]: Vertical total size[7:0]
0x3810	H_WIN_OFF	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Manual horizontal windowing offset[11:8]
0x3811	H_WIN_OFF	0x10	RW	Bit[7:0]: Manual horizontal windowing offset[7:0]

table 6-8 timing control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x3812	ISP Y WIN	0x00	RW	Bit[7:0]: isp_y_win[15:8] ISP vertical windowing offset
0x3813	ISP Y WIN	0x08	RW	Bit[7:0]: isp_y_win[7:0] ISP vertical windowing offset
0x3814	H_INC	0x11	RW	Bit[7:4]: Horizontal sub-sample odd increase number Bit[3:0]: Horizontal sub-sample odd increase number
0x3815	H_INC	0x11	RW	Bit[7:4]: Vertical sub-sample odd increase number Bit[4:0]: Vertical sub-sample even increase number
0x3816	HSYNC START	0x00	RW	Bit[7:0]: hsync_start[15:8] HSYNC start point
0x3817	HSYNC START	0x00	RW	Bit[7:0]: hsync_start[7:0] HSYNC start point
0x3818	HSYNC END	0x00	RW	Bit[7:0]: hsync_end[15:8] HSYNC end point
0x3819	HSYNC END	0x00	RW	Bit[7:0]: hsync_end[7:0] HSYNC end point
0x381A	HSYNC FIRST	0x00	RW	Bit[7:0]: hsync_first[15:8] HSYNC first active row start position
0x381B	HSYNC FIRST	0x00	RW	Bit[7:0]: hsync_first[7:0] HSYNC first active row start position
0x381C~ 0x381F	RSVD	–	–	Reserved
0x3820	FORMAT1	0x00	RW	Bit[7]: vsub48_blc Bit[6]: vflip_blc Bit[5:4]: Not used Bit[3]: byp_isp Bit[2]: Vflip Bit[1]: Vbin4 Bit[0]: Vbin2

table 6-8 timing control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x3821	FORMAT2	0x00	RW	Bit[7]: Not used Bit[6]: hdr_en[0] Works only when 0x5005[0] = 0 0: Non-HDR 1: HDR2 Bit[5]: hdr_quarter Bit[4]: hsync_en Bit[3]: fman Bit[2]: Horizontal mirror control 0: Mirrored image 1: Normal image Bit[1]: Digital hsub Bit[0]: Not used
0x3822	REG22	0x88	RW	Bit[7:5]: addr0_num Bit[4:0]: ablc_num
0x3823	REG23	0x00	RW	Bit[7]: href_flg_clr_opt Bit[6]: ext_vs_re Bit[5]: ext_vs_en Bit[4]: r_init_man Bit[3]: vts_no_latch Bit[2:0]: ablc_adj
0x3824	CS RST FSIN	0x00	RW	Bit[7:0]: cs_rst_fsin[15:8] CS reset value high byte at vs_ext
0x3825	CS RST FSIN	0x00	RW	Bit[7:0]: cs_rst_fsin[7:0] CS reset value low byte at vs_ext
0x3826	R RST FSIN	0x00	RW	Bit[7:0]: r_rst_fsin[15:8] R reset value high byte at vs_ext
0x3827	R RST FSIN	0x00	RW	Bit[7:0]: r_rst_fsin[7:0] R reset value low byte at vs_ext
0x3828	FVTS	0x00	RW	Bit[7:0]: Fvts[15:8] Fractional vertical timing size high byte unit pixel
0x3829	FVTS	0x00	RW	Bit[7:0]: Fvts[7:0] Fractional vertical timing size low byte unit pixel
0x382A	REG2A	0x04	RW	Bit[7:0]: tc_r_int_adj
0x382B	REG2B	0x16	RW	Bit[7:0]: grp_wr_start
0x382C	BLC COL ST	0x00	RW	Bit[7:0]: blc_col_st[7:0] Black column start address
0x382D	BLC COL END	0x7F	RW	Bit[7:0]: blc_col_end[7:0] Black column end address

table 6-8 timing control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x382E	CALIBRATION LINE NUM	0x0E	RW	Bit[7:5]: Not used Bit[4:0]: calibration_line_num
0x382F	TC CTRL2F	0x84	RW	Bit[7]: sof_o select option Bit[6]: r_intr_tc_en Bit[5]: r_vref_opt Bit[4]: vsync_polarity Bit[3:0]: vsync_width
0x3830	VSYNC RISING RCNT	0x00	RW	Bit[7:0]: vsync_rising_rcnt[15:8]
0x3831	VSYNC RISING RCNT	0x00	RW	Bit[7:0]: vsync_rising_rcnt[7:0]
0x3832	VSYNC RISING CCNT	0x00	RW	Bit[7:0]: vsync_rising_ccnt[15:8]
0x3833	VSYNC RISING CCNT	0x01	RW	Bit[7:0]: vsync_rising_ccnt[7:0]
0x3834	SNR H SUB	0x00	RW	Bit[7:4]: Not used Bit[3:0]: snr_h_sub
0x3835	REG35	0x04	RW	Bit[7:6]: Not used Bit[5]: byp_isp_man Bit[4]: Not used Bit[3]: vts_auto_en Bit[2]: blk_col_dis_o Bit[1:0]: r_href_w
0x3836	REG36	0x0C	RW	Bit[7:6]: Not used Bit[5:0]: ablc_use_num
0x3837	REG37	0x02	RW	Bit[7:5]: Not used Bit[4:0]: zline_use_num[5:1]
0x3838	H_AUTO_OFF_H	0x00	RW	Bit[7:5]: Not used Bit[4:0]: H_offset[12:8] for auto size mode Offset is complemental code 0x0001 is to right shift 1 pixel 0x1FFF is to left shift 1 pixel
0x3839	H_AUTO_OFF_L	0x00	RW	Bit[7:0]: H_offset[7:0] for auto size mode
0x383A	V_AUTO_OFF_H	0x00	RW	Bit[7:5]: Not used Bit[4:0]: V_offset[12:8] for auto size mode Offset is complemental code 0x0001 is to up shift 1 row 0x1FFF is to down shift 1 row
0x383B	V_AUTO_OFF_L	0x00	RW	Bit[7:0]: V_offset[7:0] for auto size mode
0x383C	BOUNDARY PIX NUM	0x00	RW	Bit[7:4]: Y boundary pixel number for auto size mode Bit[3:0]: X boundary pixel number for auto size mode

table 6-8 timing control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x383D	AUTO_SIZE_CTRL	0x00	RW	Bit[7]: add2line_en_vskip Bit[6]: Not used Bit[5]: V window auto enable Bit[4]: H window auto enable Bit[3]: V end size auto enable Bit[2]: V start size auto enable Bit[1]: H end size auto enable Bit[0]: H start size auto enable
0x383E	REG3E	0x00	RW	Bit[7:0]: intr_tc_o[15:8]
0x383F	REG3F	0x00	RW	Bit[7:0] intr_tc_o[7:0]
0x3840	REG40	0x03	RW	Bit[7:4]: ext_vsync_div Bit[3:2]: Not used Bit[1]: isp_y_win_flip_adj Bit[0]: isp_x_win_mirr_adj
0x3841	REG41	0x02	RW	Bit[7:0]: zline_tnum[9:2] Zline timing line number
0x3842	REG42	0x00	RW	Bit[7]: Not used Bit[6]: Hscale2 Bit[5]: Hscale4 Bit[4]: Hscale8 Bit[3]: Not used Bit[2]: Vscale2 Bit[1]: Vscale4 Bit[0]: Vscale8
0x3843	REG43	0x00	RW	Bit[7]: emb_token_keep Bit[6]: emb_token_1f_opt Bit[5]: emb_token_latch_opt Bit[3:0]: afc_wcnt
0x3844	REG44	0x00	RW	Bit[3:2]: grp_wr_start Bit[1:0]: tc_r_int_adj[9:8]
0x3845	REG45	0x08	RW	Bit[7:0]: extra vfpn_line_num
0x3846	REG46	0x55	RW	Bit[7:0]: emb_token0
0x3847	REG47	0xaa	RW	Bit[7:0]: emb_token1
0x3848	EMB_TOKEN0	--	R	Bit[7:0]: emb_token0_use
0x3849	EMB_TOKEN1	--	R	Bit[7:0]: emb_token1_use
0x3850	X START AUTO	–	R	Bit[7:0]: x_start_auto[15:8]
0x3851	X START AUTO	–	R	Bit[7:0]: x_start_auto[7:0]
0x3852	Y START AUTO	–	R	Bit[7:0]: y_start_auto[15:8]
0x3853	Y START AUTO	–	R	Bit[7:0]: y_start_auto[7:0]

table 6-8 timing control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x3854	X START END	–	R	Bit[7:0]: x_start_end[15:8]
0x3855	X START END	–	R	Bit[7:0]: x_start_end[7:0]
0x3856	Y START END	–	R	Bit[7:0]: y_start_end[15:8]
0x3857	Y START END	–	R	Bit[7:0]: y_start_end[7:0]
0x3858	X WIN OFF	–	R	Bit[7:0]: x_win_off[7:0]
0x3860	TC R	–	R	Bit[7:0]: tc_r[15:8]
0x3861	TC R	–	R	Bit[7:0]: tc_r[7:0]
0x3862	FRAME CNT	–	R	Bit[7:0]: frame_cnt[15:8]
0x3863	FRAME CNT	–	R	Bit[7:0]: frame_cnt[7:0]

6.9 embedded line [0x3900 - 0x3903, 0x3906 - 0x3907, 0x5C08]

table 6-9 embedded line registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3900	REG0	0x00	RW	Bit[7:6]: Reserved Bit[5]: Embedded line done interrupt clear bit Writing 1 will clear embedded line done interrupt. Writing 0 does not change status Bit[4]: SRAM violation interrupt clear bit Writing 1 will clear SRAM violation interrupt. Writing 0 does not change status Bit[3]: Embedded line done interrupt status bit Bit[2]: SRAM violation interrupt status bit Bit[1]: Embedded line done interrupt enable Bit[0]: SRAM violation interrupt enable
0x3901	REG1	0xFF	RW	Bit[7:0]: Dummy data value which will appear on image data bus when embedded line reach the length specified by registers {0x3906:0x3907}
0x3902	REG2	0xAD	RW	Bit[7:0]: Tag value
0x3903	REG3	0x00	RW	Bit[7:3]: Reserved Bit[2]: One of this bit indicates embedded line is active Bit[1]: Tag data insertion enable bit Bit[0]: Embedded line function enable bit

table 6-9 embedded line registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3906	REG6	0x00	RW	Bit[7:0]: Embedded lines total length low byte Tag data are not included in this total length
0x3907	REG7	0x00	RW	Bit[7:0]: Embedded lines total length low byte Tag data are not included in this total length
0x5C08	WIN MAN EN	0x00	RW	Bit[7:4]: Embedded line number Bit[3]: Not used Bit[2]: Embedded line position 0: At beginning of image frame 1: At end of image frame Bit[1:0]: Not used

6.10 strobe control [0x3B00, 0x3B02 - 0x3B05]

table 6-10 strobe control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3B00	STROBE CTRL	0x00	RW	Bit[7]: Strobe ON/OFF Bit[6]: Strobe polarity 0: Active high 1: Active low Bit[5:4]: width_in_xenon Bit[3]: Not used Bit[2:0]: Strobe mode 000: Xenon 001: LED1 010: LED2 011: LED3 100: LED4
0x3B02	STROBE DMY H	0x00	RW	Bit[7:0]: strobe_add_dummy[15:8] Dummy line number added at strobe high byte
0x3B03	STROBE DMY L	0x00	RW	Bit[7:0]: strobe_add_dummy[7:0] Dummy line number added at strobe low byte

table 6-10 strobe control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3B04	STROBE CTRL	0x00	RW	Bit[7:4]: Not used Bit[3]: start_point_sel Bit[2]: Strobe repeat enable Bit[1:0]: Strobe latency 00: Strobe generated at next frame 01: Delay one frame Strobe generated 2 frames later 10: Delay one frame Strobe generated 3 frames later 11: Delay one frame Strobe generated 4 frames later
0x3B05	STROBE WIDTH	0x00	RW	Bit[7:2]: Strobe pulse width step Bit[1:0]: Strobe pulse width gain strobe_pulse_width = 128×(2^gain)×(step+1)×Tsclk

6.11 illumination PWM [0x3B40 - 0x3B52]

table 6-11 illumination PWM registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3B40	P1 DLY	0x10	RW	Bit[7:5]: Not used Bit[4:0]: pulse_dly1 First pulse delay 0~31 0x00: -0.5 frame 0x1F: 0.5 frame Others: Not used
0x3B41	P2 DLY	0x10	RW	Bit[7:5]: Not used Bit[4:0]: pulse_dly2 Second pulse delay 0~31 0x00: -0.5 frame 0x1F: 0.5 frame Others: Not used

table 6-11 illumination PWM registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3B42	P3 DLY	0x10	RW	Bit[7:5]: Not used Bit[4:0]: pulse_dly3 Third pulse delay 0~31 0x00: -0.5 frame 0x1F: 0.5 frame Others: Not used
0x3B43	P4 DLY	0x10	RW	Bit[7:5]: Not used Bit[4:0]: pulse_dly4 Fourth pulse delay 0~31 0x00: -0.5 frame 0x1F: 0.5 frame Others: Not used
0x3B44	DURATION CTRL0	0x11	RW	Bit[7:4]: Duration2 Second pulse duration 0~15 frames Bit[3:0]: Duration1 First pulse duration 0~15 frames
0x3B45	DURATION CTRL1	0x11	RW	Bit[7:4]: Duration4 Fourth pulse duration 0~15 frames Bit[3:0]: Duration3 Third pulse duration 0~15 frames
0x3B46	P0 DUTY	0x1F	RW	Bit[7:5]: Not used Bit[4:0]: duty_cycle1 First pulse duty cycle 0~31
0x3B47	P1 DUTY STEP	0x1F	RW	Bit[7:5]: Not used Bit[4:0]: duty_step2 Second pulse duty cycle step
0x3B48	P2 DUTY	0x1F	RW	Bit[7:5]: Not used Bit[4:0]: duty_cycle3 Third pulse duty cycle 0~31
0x3B49	P3 DUTY STEP	0x1F	RW	Bit[7:5]: Not used Bit[4:0]: duty_step4 Fourth pulse duty cycle step
0x3B4A	GAP CTRL1	0x00	RW	Bit[7:0]: Gap1 between pulse 0 and pulse 1, 0~255 frames
0x3B4B	GAP CTRL2	0x00	RW	Bit[7:0]: Gap2 between pulse 1 and pulse 2
0x3B4C	GAP CTRL3	0x00	RW	Bit[7:0]: Gap3 between pulse 2 and pulse 3
0x3B4D	GAP CTRL4	0x00	RW	Bit[7:0]: Gap4 between pulse 3 and pulse 0

table 6-11 illumination PWM registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3B4E	PWM CTRL	0x00	RW	Bit[7]: pwm_req_r Bit[6]: Not used Bit[5]: illum_sel Bit[4]: duty_no_map Bit[3]: no_gap Bit[2]: sel_slot_out Bit[1]: Manual setting duty cycle for duration1 and duration3 Bit[0]: pwm_repeat
0x3B4F	SLOT WIDTH	0x02	RW	Bit[7:4]: Not used Bit[3:0]: slot_width_r
0x3B50	RAMP2 XSTEP	0x01	RW	Bit[7:4]: Not used Bit[3:0]: ramp2_xstep_r Second pulse duty cycle step
0x3B51	RAMPR4 XSTEP	0x01	RW	Bit[7:4]: Not used Bit[3:0]: rampr4_xstep_r Fourth pulse duty cycle step
0x3B52	TAIL DUTY CYCLE	0x80	RW	Bit[7]: end_opt 0: No pulse when PWM ends 1: Free running at pre-defined duty cycle Bit[6]: tail_stop_toggle Bit[5]: Not used Bit[4:0]: duty_tail Tail pulse duty cycle step

6.12 UART control [0x3C00 - 0x3C0B, 0x3C10 - 0x3C11, 0x3C22, 0x3C30 - 0x3C33]

table 6-12 UART control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3C00	R0	–	R	Bit[7:6]: Not used Bit[5]: Transmit enable Bit[4]: Receive enable Bit[3]: Transmit parity enable Bit[2]: Receive parity enable Bit[1]: Clear receive operation Bit[0]: Clear transmit operation

table 6-12 UART control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3C01	R1	–	R	Bit[7:4]: Receive FIFO almost full counter Bit[3:0]: Receive FIFO almost empty counter
0x3C02	R2	–	R	Bit[7:4]: Transmit FIFO almost full counter Bit[3:0]: Transmit FIFO almost empty counter
0x3C03	R3	–	R	Bit[7:0]: Receive dividing coefficient[7:0]
0x3C04	R4	–	R	Bit[7:0]: Transmit dividing coefficient[7:0]
0x3C05	R5	–	R	Bit[7:6]: Receive parity select Bit[5:4]: Transmit parity select Bit[3]: Transmit break enable Bit[2]: Address match automatic check enable Bit[1]: Transmit address bit enable Bit[0]: Receive address bit enable
0x3C06	R6	–	R	Bit[7:0]: UART receive address
0x3C07	R7	–	R	Bit[7:0]: UART broadcast address
0x3C08	R8	–	R	Bit[7:6]: Not used Bit[5:3]: Receive data bit width Bit[2:0]: Transmit data bit width
0x3C09	R9	–	R	Bit[7:4]: Not used Bit[3:2]: Receive stop bit width Bit[1:0]: Transmit stop bit width
0x3C0A	R3	–	R	Bit[7:0]: Receive dividing coefficient[15:8]
0x3C0B	R4	–	R	Bit[7:0]: Transmit dividing coefficient[15:8]
0x3C10	R10	–	R	Bit[7:0]: Transmit data bits
0x3C11	R11	–	R	Bit[7:1]: Not used Bit[0]: Transmit address bit
0x3C22	R22	–	R	Bit[7:4]: Receive FIFO status Bit[3:0]: Transmit FIFO status
0x3C30	R30	–	R	Bit[7:3]: Not used Bit[2:0]: Error interrupt enable
0x3C31	R31	–	R	Bit[7:0]: FIFO status interrupt enable
0x3C32	R32	–	R	Bit[7:3]: Not used Bit[2:0]: Error interrupt clear (W) and status (R)
0x3C33	R33	–	R	Bit[7:0]: FIFO status interrupt clear (W) and status (R)

6.13 OTP control [0x3D80 - 0x3D8D, 0x3D92, 0x7000 - 0x79FF]

table 6-13 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3D80	OTP_PROGRAM_CTRL	0x00	RW	Bit[7]: OTP_wr_busy (read only) Bit[6:1]: Not used Bit[0]: OTP_program_enable (write only)
0x3D81	OTP_LOAD_CTRL	0x00	RW	Bit[7]: OTP_rd_busy (read only) Bit[6]: Not used Bit[5]: OTP_bist_error (read only) Bit[4]: OTP_bist_done (read only) Bit[3:1]: Not used Bit[0]: OTP_load_enable
0x3D82	R PGM PULSE	0x2E	RW	Bit[7:0]: Control program strobe pulse[7:0], by 8×Tsclk
0x3D83	R LOAD PULSE	0x12	RW	Bit[7:6]: Control program strobe pulse[9:8], by 8×Tsclk Bit[5:0]: Control load strobe pulse, by Tsclk
0x3D84	OTP_MODE_CTRL	0x80	RW	Bit[7]: Program disable 1: Disable Bit[6]: Mode select 0: Auto mode 1: Manual mode Bit[5:0]: Not used
0x3D85	OTP_REG85	0x13	RW	Bit[7:6]: Not used Bit[5]: OTP_bist_select 0: Compare with SRAM 1: Compare with zero Bit[4]: OTP_bist_enable Bit[3]: Not used Bit[2]: OTP power up load data enable Bit[1]: OTP power up load setting enable Bit[0]: OTP write register load setting enable
0x3D86	SRAM TEST SIGNALS	0x01	RW	Bit[7]: Not used Bit[6]: r_rst_otp_o Bit[5]: r_rme Bit[4]: r_test Bit[3:0]: r_rm
0x3D87	R PS2CS	0x6C	RW	Bit[7:4]: PGS to PGENB Bit[3:0]: PS to CSB time control, by sclk
0x3D88	OTP_START_ADDRESS	0x00	RW	OTP Start High Address for Manual Mode
0x3D89	OTP_START_ADDRESS	0x00	RW	OTP Start Low Address for Manual Mode

table 6-13 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3D8A	OTP_END_ADDRESS	0x00	RW	OTP End High Address For Manual Mode
0x3D8B	OTP_END_ADDRESS	0x00	RW	OTP End Low Address For Manual Mode
0x3D8C	OTP_SETTING_STT_ ADDRESS	0x00	RW	OTP Start High Address For Load Setting
0x3D8D	OTP_SETTING_STT_ ADDRESS	0x00	RW	OTP Start Low Address For Load Setting
0x3D8E	OTP_BIST_ERR_ ADDRESS	–	R	OTP Check Error Address High
0x3D8F	OTP_BIST_ERR_ ADDRESS	–	R	OTP Check Error Address Low
0x3D90	OTP STROBE GAP	0x18	RW	Bit[7:0]: otp_strobe_gap_pgm Gap between strobe pulse when pgm × 8
0x3D91	OTP STROBE GAP	0x06	RW	Bit[7:0]: otp_strobe_gap_load Gap between strobe pulse when load × 8
0x3D92	PGST2PS	0x2A	RW	Bit[7:4]: cs2psend Bit[3:0]: pgst2ps, by sclk
0x6000~ 0x77FF	OTP_SRAM	0x00	RW	Bit[7:0]: OTP buffer

6.14 FREX control [0x3F85 - 0x3F87, 0x3F89 - 0x3F93, 0x3F9E - 0x3F9F]

table 6-14 FREX strobe control registers (sheet 1 of 3)

address	register name	default value	R/W	description
0x3F85	FREX REG5	0x00	RW	Bit[7:0]: Frame exposure[23:16] MSB of frame exposure time in mode 2 Exposure time in units of 128 system clock cycles
0x3F86	FREX REG6	0x00	RW	Bit[7:0]: Frame exposure[15:8] Middle byte of frame exposure time in mode 2
0x3F87	FREX REG7	0x05	RW	Bit[7:0]: Frame exposure[7:0] LSB of frame exposure in mode 2

table 6-14 FREX strobe control registers (sheet 2 of 3)

address	register name	default value	R/W	description
0x3F89	FREX REG9	0x00	RW	Bit[3:0]: strobe_width[19:16] MSB of strobe width in mode 2. Strobe width in units of 1 system clock cycle
0x3F8A	FREX REGA	0x06	RW	Bit[7:0]: strobe_width[15:8] Middle byte of strobe width in mode 2
0x3F8B	FREX REGB	0x00	RW	Bit[7:0]: strobe_width[7:0] LSB of strobe width in mode 2
0x3F8C	FREX REGC	0x00	RW	Bit[7:5]: Not used Bit[4:0]: shutter_dly[12:8] MSB of shutter delay in mode 2 Shutter delay is in units of 128 system clock cycles
0x3F8D	FREX REGD	0x44	RW	Bit[7:0]: shutter_dly[7:0] LSB of shutter delay in mode 2
0x3F8E	FREX REGE	0x1F	RW	Bit[7:0]: frex_pre_charge_width[15:8] MSB of sensor precharge in mode 2 Sensor precharge is in units of 1 system clock cycles
0x3F8F	FREX REGF	0x40	RW	Bit[7:0]: frex_pre_charge_width[7:0] LSB of sensor precharge in mode 2
0x3F90	FREX REG10	0x00	RW	Bit[7:0]: Readout delay[15:8] MSB of readout delay time in mode 2 Readout delay time is in units of 128 system clock cycles
0x3F91	FREX REG11	0x01	RW	Bit[7:0]: Readout delay[7:0] LSB of readout delay time in mode 2
0x3F92	FREX_REG12	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Strobe delay[12:8] MSB of strobe delay time
0x3F93	FREX_REG13	0x00	RW	Bit[7:0]: Strobe delay[7:0] LSB of strobe delay time
0x3F9E	FREX REG1E	0x01	RW	Bit[7:1]: Not used Bit[0]: frex_sccb_req_repeat_trig_sel 0: SOF 1: EOF

table 6-14 FREX strobe control registers (sheet 3 of 3)

address	register name	default value	R/W	description
0x3F9F	FREX REG1F	0x04	RW	Bit[7]: frex_sccb_req Self clearing Bit[6]: Not used Bit[5]: frex_strobe_out_sel 0: Strobe for rolling mode 1: Strobe for frame mode Bit[4]: frex_nopchg Bit[3]: frex_strobe polarity 0: Active high 1: Active low Bit[2]: frex_shutter polarity 0: Active high 1: Active low Bit[1]: frex_pad_in_enable 0: Frame mode is triggered by register 1: Frame mode is triggered by FREX pad Bit[0]: no_latch at SOF for frex_sccb_req 0: Trigger frame mode in SOF 1: Trigger frame mode immediately

6.15 PSRAM control [0x3F00 - 0x3F03, 0x3F0E - 0x3F0F]

table 6-15 PSRAM control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3F00	PSRAM REG0	0x10	RW	Bit[7]: sread_st_opt 0: Manual mode 1: At asp_start Bit[6]: sread_d1r Bit[5:4]: ady_inc Bit[3]: rrblue_re Bit[2]: reven_re Bit[1]: srclk_re Bit[0]: srclk_d2
0x3F01	PSRAM REG1	0x00	RW	Bit[7:0]: sread_man_st_pt[15:8]
0x3F02	PSRAM REG2	0x00	RW	Bit[7:0]: sread_mam_st_pt[7:0]
0x3F03	PSRAM REG3	0x03	RW	Bit[7:0]: Not used Bit[1]: sread_opt Bit[0]: srclk_fullspeed in vbin mode

table 6-15 PSRAM control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x3F0E	SRAM READPOINT	–	R	Bit[7:0]: sram_readpoint[15:8] SRAM readout point at CS high byte
0x3F0F	SRAM READPOINT	–	R	Bit[7:0]: sram_readpoint[7:0] SRAM readout point at CS low byte

6.16 BLC control [0x4000 - 0x401A, 0x4020 - 0x40BF]

table 6-16 BLC control registers (sheet 1 of 11)

address	register name	default value	R/W	description
0x4000	BLC CTRL00	0x13	RW	Bit[7]: r_img_gfirst_rvs Bit[6]: Vertical flip black lines enable 0: Normal 1: Vertical flip Bit[5]: r_img_rblue_rvs Bit[4]: r_dc_man Set 1-channel BLC DC offset manually Bit[3]: target_adj_dis Disable adjust final applied target Bit[2]: cmp_en Compensation enable by adding color channel difference when using 1-channel BLC Bit[1]: dither_en Dithering enable Bit[0]: mf_en Median filter enable
0x4001	BLC CTRL01	0x60	RW	Bit[7]: gain_trig_beh Bit[6]: format_trig_beh Bit[5]: kcoef_man_en Set dark current coefficient manually Bit[4]: off_man_en Set BLC offset manually Bit[3]: zero_ln_out_en Zero line output enable Bit[2]: blk_ln_out_en Black line output enable Bit[1:0]: byp_mode No black offset will be applied on image

table 6-16 BLC control registers (sheet 2 of 11)

address	register name	default value	R/W	description
0x4002	BLK LVL TARGET	0x00	RW	Bit[7:2]: Not used Bit[1:0]: blk_lvl_target[9:8] BLC target high 2 bits
0x4003	BLK LVL TARGET	0x10	RW	Bit[7:0]: blk_lvl_target[7:0] BLC target low 8 bits
0x4004	HWIN OFF	0x00	RW	Bit[7:4]: Not used Bit[3:0]: hwin_off[11:8] Left boundary of BLC window high 4 bits
0x4005	HWIN OFF	0x04	RW	Bit[7:0]: hwin_off[7:0] Left boundary of BLC window low 8 bits
0x4006	HWIN PAD	0x00	RW	Bit[7:4]: Not used Bit[3:0]: hwin_pad[11:8] Right boundary of BLC window high 4 bits
0x4007	HWIN PAD	0x04	RW	Bit[7:0]: hwin_pad[7:0] Right boundary of BLC window low 8 bits
0x4008	BLC CTRL08	0x00	RW	Bit[7:0]: bl_start Black line start position
0x4009	BLC CTRL09	0x09	RW	Bit[7:0]: bl_end Black line end position
0x400A	OFF LIM TH	0x02	RW	Bit[7:0]: off_lim_th[15:8] Threshold for the difference between difference channels in the same frame high 8 bits (works only when register 0x4000[3] = 0)
0x400B	OFF LIM TH	0x00	RW	Bit[7:0]: off_lim_th[7:0] Threshold for the difference between difference channels in the same frame low 8 bits (works only when register 0x4000[3] = 0)
0x400C~ 0x400D	NOT USED	–	–	Not Used
0x400E	BLC CTRL0E	0x00	RW	Bit[7:0]: mf_th Median filter threshold in black line

table 6-16 BLC control registers (sheet 3 of 11)

address	register name	default value	R/W	description
0x400F	BLC CTRL0F	0x80	RW	Bit[7]: r_exp_chg_trig_en Exposure BLC trigger enable Bit[6]: Debug mode Bit[5:4]: Not used Bit[3]: r_v15_one_channel Pure 1-channel BLC enable Bit[2]: r_en_adp_k Enable adaptive K by average Bit[1]: r_dc_offset_mode Add offset in zero line in 1-channel BLC Bit[0]: r_compute_offset_v15 1-channel BLC enable (black line from whole frame, zero line by channel)
0x4010	BLC CTRL10	0xF0	RW	Bit[7]: off_trig_en Offset BLC trigger enable Bit[6]: gain_chg_trig_en Gain change BLC trigger enable Bit[5]: fmt_chg_trig_en Format change BLC trigger enable Bit[4]: rst_trig_en Reset BLC trigger enable Bit[3]: man_avg_en BLC average in V BLC manual trigger (works only when register 0x4010[2] = 1) Bit[2]: man_trig Manual BLC trigger enable Bit[1]: off_frz_en BLC freeze enable Bit[0]: off_always_up BLC always update enable

table 6-16 BLC control registers (sheet 4 of 11)

address	register name	default value	R/W	description
0x4011	BLC CTRL11	0xFF	RW	Bit[7]: r_off_cmp_man_en Offset compensation manual enable (works only when register 0x4000[2] = 1) Bit[6]: off_chg_multi-frame_en Offset BLC multi-frame trigger enable Bit[5]: fmt_chg_multi-frame_en Format change BLC multi-frame trigger enable Bit[4]: gain_chg_multi-frame_en Gain change BLC multi-frame trigger enable Bit[3]: rst_multi-frame_mode Reset BLC multi-frame trigger enable Bit[2]: off_chg_multi-frame_mode Offset change multi-frame BLC mode 0: Current frame BLC value 1: Weighted multi-frame BLC value Bit[1]: fmt_chg_multi-frame_mode Format change multi-frame BLC mode 0: Current frame BLC value 1: Weighted multi-frame BLC value Bit[0]: gain_chg_multi-frame_mode Gain change multi-frame BLC mode 0: Current frame BLC value 1: Weighted multi-frame BLC value
0x4012	BLC CTRL12	0x08	RW	Bit[7:0]: rst_trig_fn Number of BLC update frames with reset trigger
0x4013	BLC CTRL13	0x02	RW	Bit[7:0]: fmt_trig_fn Number of BLC update frames with format change trigger
0x4014	BLC CTRL14	0x02	RW	Bit[7:0]: gain_trig_fn Number of BLC update frames with gain change trigger
0x4015	BLC CTRL15	0x02	RW	Bit[7:0]: off_trig_fn Number of BLC update frames with offset trigger
0x4016	OFF TRIG TH	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_trig_th[9:8] Threshold of offset trigger high 2 bits
0x4017	OFF TRIG TH	0x04	RW	Bit[7:0]: off_trig_th[7:0] Threshold of offset trigger low 8 bits

table 6-16 BLC control registers (sheet 5 of 11)

address	register name	default value	R/W	description
0x4018	BLC CTRL18	0x00	RW	Bit[7]: r_blk_col_auto Enable mini-row auto ON/OFF mode (works only when register 0x4018[3]=1) Bit[6]: r_col_one_ch_o Enable mini-row in 1-channel BLC (works only when register 0x4018[3]=1) Bit[5]: r_blk_col_out_en Enable mini-row output (works only when register 0x4018[3]=1) Bit[4]: r_blk_col_4ch_en Enable mini-row in normal BLC mode (works only when register 0x4018[3]=1) Bit[3]: r_blk_col_en Mini-row enable Bit[2:0]: Not used
0x4019	BLC CTRL19	0x04	RW	Bit[7:0]: r_blk_ln_num Black input line number (works only when register 0x401A[2] = 1)
0x401A	BLC CTRL1A	0x40	RW	Bit[7]: Not used Bit[6]: r_kcoef_mirror Auto K adjustment with mirror on/off Bit[5]: r_adp_dc_switch_en Enable 1-channel BLC to 4-channel BLC auto switch if DC is high Bit[4]: Debug mode Bit[3]: r_vfpn_en Enable BLC to VFPN cancellation Bit[2]: r_ln_man Black input line manual mode Bit[1]: hdr_nsft BLC for 4-exposure HDR Bit[0]: hdr_en BLC for HDR enable
0x4020	BLC CTRL20	0x00	RW	Bit[7:0]: off_cmp_th0000 Works only when register 0x4011[7] = 1
0x4021	BLC CTRL21	0x00	RW	Bit[7:0]: off_cmp_k0000 Works only when register 0x4011[7] = 1
0x4022	BLC CTRL22	0x00	RW	Bit[7:0]: off_cmp_th0001 Works only when register 0x4011[7] = 1
0x4023	BLC CTRL23	0x00	RW	Bit[7:0]: off_cmp_k0001 Works only when register 0x4011[7] = 1
0x4024	BLC CTRL24	0x00	RW	Bit[7:0]: off_cmp_th0010 Works only when register 0x4011[7] = 1
0x4025	BLC CTRL25	0x00	RW	Bit[7:0]: off_cmp_k0010 Works only when register 0x4011[7] = 1

table 6-16 BLC control registers (sheet 6 of 11)

address	register name	default value	R/W	description
0x4026	BLC CTRL26	0x00	RW	Bit[7:0]: off_cmp_th0011 Works only when register 0x4011[7] = 1
0x4027	BLC CTRL27	0x00	RW	Bit[7:0]: off_cmp_k0011 Works only when register 0x4011[7] = 1
0x4028	BLC CTRL28	0x00	RW	Bit[7:0]: off_cmp_th0100 Works only when register 0x4011[7] = 1
0x4029	BLC CTRL29	0x00	RW	Bit[7:0]: off_cmp_k0100 Works only when register 0x4011[7] = 1
0x402A	BLC CTRL2A	0x00	RW	Bit[7:0]: off_cmp_th0101 Works only when register 0x4011[7] = 1
0x402B	BLC CTRL2B	0x00	RW	Bit[7:0]: off_cmp_k0101 Works only when register 0x4011[7] = 1
0x402C	BLC CTRL2C	0x00	RW	Bit[7:0]: off_cmp_th0110 Works only when register 0x4011[7] = 1
0x402D	BLC CTRL2D	0x00	RW	Bit[7:0]: off_cmp_k0110 Works only when register 0x4011[7] = 1
0x402E	BLC CTRL2E	0x00	RW	Bit[7:0]: off_cmp_th0111 Works only when register 0x4011[7] = 1
0x402F	BLC CTRL2F	0x00	RW	Bit[7:0]: off_cmp_k011 Works only when register 0x4011[7] = 1
0x4030	BLC CTRL30	0x00	RW	Bit[7:0]: off_cmp_th1000 Works only when register 0x4011[7] = 1
0x4031	BLC CTRL31	0x00	RW	Bit[7:0]: off_cmp_k1000 Works only when register 0x4011[7] = 1
0x4032	BLC CTRL32	0x00	RW	Bit[7:0]: off_cmp_th1001 Works only when register 0x4011[7] = 1
0x4033	BLC CTRL33	0x00	RW	Bit[7:0]: off_cmp_k1001 Works only when register 0x4011[7] = 1
0x4034	BLC CTRL34	0x00	RW	Bit[7:0]: off_cmp_th1010 Works only when register 0x4011[7] = 1
0x4035	BLC CTRL35	0x00	RW	Bit[7:0]: off_cmp_k1010 Works only when register 0x4011[7] = 1
0x4036	BLC CTRL36	0x00	RW	Bit[7:0]: off_cmp_th1011 Works only when register 0x4011[7] = 1
0x4037	BLC CTRL37	0x00	RW	Bit[7:0]: off_cmp_k1011 Works only when register 0x4011[7] = 1
0x4038	BLC CTRL38	0x00	RW	Bit[7:0]: off_cmp_th1100 Works only when register 0x4011[7] = 1

table 6-16 BLC control registers (sheet 7 of 11)

address	register name	default value	R/W	description
0x4039	BLC CTRL39	0x00	RW	Bit[7:0]: off_cmp_k1100 Works only when register 0x4011[7] = 1
0x403A	BLC CTRL3A	0x00	RW	Bit[7:0]: off_cmp_th1101 Works only when register 0x4011[7] = 1
0x403B	BLC CTRL3B	0x00	RW	Bit[7:0]: off_cmp_k1101 Works only when register 0x4011[7] = 1
0x403C	BLC CTRL3C	0x00	RW	Bit[7:0]: off_cmp_th1110 Works only when register 0x4011[7] = 1
0x403D	BLC CTRL3D	0x00	RW	Bit[7:0]: off_cmp_k1110 Works only when register 0x4011[7] = 1
0x403E	BLC CTRL3E	0x00	RW	Bit[7:0]: off_cmp_th1111 Works only when register 0x4011[7] = 1
0x403F	BLC CTRL3F	0x00	RW	Bit[7:0]: off_cmp_k1111 Works only when register 0x4011[7] = 1
0x4040	OFF MAN0000	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0000[9:8] Works only when register 0x4001[4] = 1
0x4041	OFF MAN0000	0x00	RW	Bit[7:0]: off_man0000[7:0] Works only when register 0x4001[4] = 1
0x4042	OFF MAN0001	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0001[9:8] Works only when register 0x4001[4] = 1
0x4043	OFF MAN0001	0x00	RW	Bit[7:0]: off_man0001[7:0] Works only when register 0x4001[4] = 1
0x4044	OFF MAN0010	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0010[9:8] Works only when register 0x4001[4] = 1
0x4045	OFF MAN0010	0x00	RW	Bit[7:0]: off_man0010[7:0] Works only when register 0x4001[4] = 1
0x4046	OFF MAN0011	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0011[9:8] Works only when register 0x4001[4] = 1
0x4047	OFF MAN0011	0x00	RW	Bit[7:0]: off_man0011[7:0] Works only when register 0x4001[4] = 1
0x4048	OFF MAN0100	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0100[9:8] Works only when register 0x4001[4] = 1
0x4049	OFF MAN0100	0x00	RW	Bit[7:0]: off_man0100[7:0] Works only when register 0x4001[4] = 1

table 6-16 BLC control registers (sheet 8 of 11)

address	register name	default value	R/W	description
0x404A	OFF MAN0101	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0101[9:8] Works only when register 0x4001[4] = 1
0x404B	OFF MAN0101	0x00	RW	Bit[7:0]: off_man0101[7:0] Works only when register 0x4001[4] = 1
0x404C	OFF MAN0110	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0110[9:8] Works only when register 0x4001[4] = 1
0x404D	OFF MAN0110	0x00	RW	Bit[7:0]: off_man0110[7:0] Works only when register 0x4001[4] = 1
0x404E	OFF MAN0111	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man0111[9:8] Works only when register 0x4001[4] = 1
0x404F	OFF MAN0111	0x00	RW	Bit[7:0]: off_man0111[7:0] Works only when register 0x4001[4] = 1
0x4050	BLC CTRL50	0x00	RW	Bit[7:0]: zl_start Zero line start position
0x4051	BLC CTRL51	0x01	RW	Bit[7:0]: zl_end Zero line end position
0x4052	KCOEF B MAN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_b_man[9:8] K for B in manual mode high 2 bits (works only when register 0x4001[5] = 1)
0x4053	KCOEF B MAN	0x00	RW	Bit[7:0]: kcoef_b_man[7:0] K for B in manual mode low 8 bits (works only when register 0x4001[5] = 1)
0x4054	KCOEF GB MAN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_gb_man[9:8] K for Gb in manual mode high 2 bits (works only when register 0x4001[5] = 1)
0x4055	KCOEF GB MAN	0x00	RW	Bit[7:0]: kcoef_gb_man[7:0] K for Gb in manual mode low 8 bits (works only when register 0x4001[5] = 1)
0x4056	KCOEF GR MAN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_gr_man[9:8] K for Gr in manual mode high 2 bits (works only when register 0x4001[5] = 1)
0x4057	KCOEF GR MAN	0x00	RW	Bit[7:0]: kcoef_gr_man[7:0] K for Gr in manual mode low 8 bits (works only when register 0x4001[5] = 1)

table 6-16 BLC control registers (sheet 9 of 11)

address	register name	default value	R/W	description
0x4058	KCOEF R MAN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: kcoef_r_man[9:8] K for R in manual mode high 2 bits (works only when register 0x4001[5] = 1)
0x4059	KCOEF R MAN	0x00	RW	Bit[7:0]: kcoef_r_man[7:0] K for R in manual mode low 8 bits (works only when register 0x4001[5] = 1)
0x405A	BLC CTRL5A	0x30	RW	Bit[7:0]: r_dc_th_1_0 Dark current threshold (works only when register 0x401A[5] = 1)
0x405B	BLC CTRL5B	0x18	RW	Bit[7:0]: r_dc_th_2_0 Dark current threshold (works only when register 0x401A[5] = 1)
0x405C	BLC CTRL5C	0x00	RW	Bit[7:6]: Not used Bit[5:0]: avg_weight for current frame Weight for multi-frame BLC
0x405D	RND GAIN TH	0x00	RW	Bit[7:2]: Not used Bit[1:0]: rnd_gain_th[9:8] Gain threshold for dithering high 2 bits (works only when register 0x4000[1] = 1)
0x405E	RND GAIN TH	0x00	RW	Bit[7:0]: rnd_gain_th[7:0] Gain threshold for dithering low 8 bits (works only when register 0x4000[1] = 1)
0x405F	BLC CTRL5F	0x00	RW	Bit[7:0]: r_dc_th_1_1 Dark current threshold (works only when register 0x401A[5] = 1)
0x4060	BLC CTRL60	0x00	RW	Bit[7:0]: r_dc_th_2_1 Dark current threshold (works only when register 0x401A[5] = 1)
0x4061	BLC CTRL61	0x00	RW	Bit[7:0]: r_dc_th_1_2 Dark current threshold (works only when register 0x401A[5] = 1)
0x4062	BLC CTRL62	0x00	RW	Bit[7:0]: r_dc_th_2_2 Dark current threshold (works only when register 0x401A[5] = 1)
0x4063	BLC CTRL63	0x00	RW	Bit[7:0]: r_dc_th_1_3 Dark current threshold (works only when register 0x401A[5] = 1)
0x4064	BLC CTRL64	0x00	RW	Bit[7:0]: r_dc_th_2_3 Dark current threshold (works only when register 0x401A[5] = 1)

table 6-16 BLC control registers (sheet 10 of 11)

address	register name	default value	R/W	description
0x4065	ZERO LN NUM	0x00	RW	Bit[7:2]: Not used Bit[1:0]: zero_ln_num[9:8] Zero line number high 2 bits
0x4066	ZERO LN NUM	0x02	RW	Bit[7:0]: zero_ln_num[7:0] Zero line number low 8 bits
0x4067	COL WIN	0x18	RW	Bit[7:0]: col_win Right boundary for mini-row
0x4068	R COL LOW GAIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: r_col_low_gain[9:8] Low gain in mini-row threshold high 2 bits (works only when register 0x4018[7]=1)
0x4069	R COL LOW GAIN	0x20	RW	Bit[7:0]: r_col_low_gain[7:0] Low gain in mini-row threshold low 8 bits (works only when register 0x4018[7]=1)
0x406A	R COL HIGH GAIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: r_col_high_gain[9:8] High gain in mini-row threshold high 2 bits (works only when register 0x4018[7]=1)
0x406B	R COL HIGH GAIN	0x40	RW	Bit[7:0]: r_col_high_gain[7:0] High gain in mini-row threshold low 8 bits (works only when register 0x4018[7]=1)
0x406C	BLC CTRL6C	0x02	RW	Bit[7:3]: Not used Bit[2:0]: r_col_div_cnt
0x406D	BLC CTRL6D	0x00	RW	Bit[7:0]: mf_col_th Median filter threshold in mini-row
0x406E	BLC CTRL6E	0x00	RW	Bit[7:0]: h_size_man[15:8]
0x406F	BLC CTRL6F	0x00	RW	Bit[7:0]: h_size_man[7:0]
0x4070~ 0x40AF	DEBUG MODE	–	R	Debug Mode
0x40B0	OFF MAN1000	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1000[9:8] Works only when register 0x4001[4] = 1
0x40B1	OFF MAN1000	0x00	RW	Bit[7:0]: off_man1000[7:0] Works only when register 0x4001[4] = 1
0x40B2	OFF MAN1001	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1001[9:8] Works only when register 0x4001[4] = 1
0x40B3	OFF MAN1001	0x00	RW	Bit[7:0]: off_man1001[7:0] Works only when register 0x4001[4] = 1

table 6-16 BLC control registers (sheet 11 of 11)

address	register name	default value	R/W	description
0x40B4	OFF MAN1010	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1010[9:8] Works only when register 0x4001[4] = 1
0x40B5	OFF MAN1010	0x00	RW	Bit[7:0]: off_man1010[7:0] Works only when register 0x4001[4] = 1
0x40B6	OFF MAN1011	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1011[9:8] Works only when register 0x4001[4] = 1
0x40B7	OFF MAN1011	0x00	RW	Bit[7:0]: off_man1011[7:0] Works only when register 0x4001[4] = 1
0x40B8	OFF MAN1100	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1100[9:8] Works only when register 0x4001[4] = 1
0x40B9	OFF MAN1100	0x00	RW	Bit[7:0]: off_man1100[7:0] Works only when register 0x4001[4] = 1
0x40BA	OFF MAN1101	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1101[9:8] Works only when register 0x4001[4] = 1
0x40BB	OFF MAN1101	0x00	RW	Bit[7:0]: off_man1101[7:0] Works only when register 0x4001[4] = 1
0x40BC	OFF MAN1110	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1110[9:8] Works only when register 0x4001[4] = 1
0x40BD	OFF MAN1110	0x00	RW	Bit[7:0]: off_man1110[7:0] Works only when register 0x4001[4] = 1
0x40BE	OFF MAN1111	0x00	RW	Bit[7:2]: Not used Bit[1:0]: off_man1111[9:8] Works only when register 0x4001[4] = 1
0x40BF	OFF MAN1111	0x00	RW	Bit[7:0]: off_man1111[7:0] Works only when register 0x4001[4] = 1

6.17 ISP frame counter [0x4900 - 0x4905]

table 6-17 ISP frame counter control registers

address	register name	default value	R/W	description
0x4900	R0	0x00	RW	Bit[7:3]: Not used Bit[2]: fcnt_eof_sel Bit[1]: fcnt_mask_dis Bit[0]: fcnt_reset
0x4901	R1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_on_number
0x4902	R2	0x00	RW	Bit[7:4]: Not used Bit[3:0]: frame_off_number
0x4903	R3	0x00	RW	Bit[7]: Not used Bit[6]: rblue_mask_dis Bit[5]: data_mask_dis Bit[4]: valid_mask_dis Bit[3]: href_mask_dis Bit[2]: eof_mask_dis Bit[1]: sof_mask_dis Bit[0]: all_mask_dis
0x4904	R4	0x09	RW	Bit[7]: href_mask_dis Bit[6]: Not used Bit[5:0]: href_mask_st
0x4905	R5	0x00	RW	Bit[7:6: Not used Bit[5:0]: href_mask_end

6.18 test control [0x4300 - 0x430D]

table 6-18 test control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4300	TEST B	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_b[11:8]
0x4301	TEST B	0x00	RW	Bit[7:0]: test_b[7:0]
0x4302	TEST GB	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_gb[11:8]
0x4303	TEST GB	0x00	RW	Bit[7:0]: test_gb[7:0]

table 6-18 test control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4304	TEST GR	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_gr[11:8]
0x4305	TEST GR	0x00	RW	Bit[7:0]: test_gr[7:0]
0x4306	TEST R	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_r[11:8]
0x4307	TEST R	0x00	RW	Bit[7:0]: test_r[7:0]
0x4308	TEST MODE	0x00	RW	Bit[7:6]: Not used Bit[5:3]: r_bit_swap Bit[2]: r_pn9_bit_rev Bit[1]: pn9_en Bit[0]: fix_color_en
0x4309	TEST W	0x00	RW	Bit[7:4]: Not used Bit[3:0]: test_w[11:8]
0x430A	TEST W	0x00	RW	Bit[7:0]: test_w[7:0]
0x430B	CLIP MAX HI	0xFF	RW	Bit[7:0]: clip_max[11:4]
0x430C	CLIP MIN HI	0x00	RW	Bit[7:0]: clip_min[11:4]
0x430D	CLIP MAX MIN LO	0xF0	RW	Bit[7:4]: clip_max[3:0] Bit[3:0]: clip_min[3:0]

6.19 ADC sync control [0x4500 - 0x4509]

table 6-19 ADC sync control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4500	CTRL	0x52	RW	Bit[7:4]: FIFO read delay Bit[3:1]: chn_man Bit[0]: srclk_inv
0x4501	R1	0x38	RW	Bit[7]: byp_sync_fifo Bit[6]: swap_en Bit[5]: vbin_avg Bit[4]: disable_gray2bin Bit[3]: hbin_avg Bit[2]: bin_en Bit[1:0]: rawout_sw

table 6-19 ADC sync control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4502	R2	0x06	RW	Bit[7]: sram_RME Bit[6]: r_fifo_swap_opt Bit[5]: rblue_re Bit[4]: Test Bit[3:0]: RM
0x4503	R3	0x00	RW	Bit[7:4]: dly_adj_o Bit[3]: fifo_clk_dis_o Bit[2]: Not used Bit[1]: hdr_nsft_o Bit[0]: sync_fifo_sof_sel
0x4504~ 0x4508	DEBUG MODE	–	–	Debug Mode
0x4509	R9	0x07	RW	Bit[7:4]: Not used Bit[3]: skip_opt Bit[2]: sfifo_ch_fix_o Bit[1]: rblue_man_en Bit[0]: rblue_man

6.20 VFIFO control [0x4600 - 0x4605]

table 6-20 VFIFO control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x4600	R VFIFO READ START	0x01	RW	Bit[7:0]: r_vfifo_read_start[15:8]
0x4601	R VFIFO READ START	0x04	RW	Bit[7:0]: r_vfifo_read_start[7:0]
0x4602	R2	0x02	RW	Bit[7:4]: r_rm Bit[3]: r_test1 Bit[2]: Not used Bit[1]: Frame reset enable Bit[0]: RAM bypass enable
0x4603	R3	0x00	RW	Bit[7:4]: start_opt Bit[3]: fix_hsize Bit[2]: fo_rd_en_wr_cnd Bit[1]: sram_rme Bit[0]: man_start_mode

table 6-20 VFIFO control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x4604	R4	–	R	Bit[7:4]: Not used Bit[3]: ram_full Bit[2]: ram_empty Bit[1]: fo_full Bit[0]: fo_empty
0x4605	R5	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Ready low tp number

6.21 PDFIFO control [0x4640 - 0x4645]

table 6-21 PDFIFO control registers

address	register name	default value	R/W	description
0x4640	PD FIFO CONTROL	0x00	RW	Bit[7:0]: PD data max number high byte/8 in one package
0x4641	PD FIFO CONTROL	0x1E	RW	Bit[7:0]: PD data max number low byte/8 in one package
0x4642	R2	0x12	RW	Bit[7:4]: r_rm Bit[3]: r_test1 Bit[2]: Not used Bit[1]: Frame reset enable Bit[0]: RAM bypass enable
0x4643	R3	0x00	RW	Bit[7:4]: start_opt Bit[3]: fix_hsize Bit[2]: fo_rd_en_wr_cnd Bit[1]: sram_rme Bit[0]: man_start_mode
0x4644	R4	–	R	Bit[7:4]: Not used Bit[3]: ram_full Bit[2]: ram_empty Bit[1]: fo_full Bit[0]: fo_empty
0x4645	R5	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Ready low tp number

6.22 MIPI control [0x4800 - 0x4809, 0x4810 - 0x48A1, 0x48B6 - 0x48BA]

table 6-22 MIPI control registers (sheet 1 of 14)

address	register name	default value	R/W	description
0x4800	MIPI CTRL00	0x04	RW	Bit[7]: Not used 1: MIPI always high speed mode Bit[6]: Not used Bit[5]: gate_sc_en 0: Clock lane is free running 1: Gate clock lane when there is no packet to transmit Bit[4]: line_sync_en 0: Do not send line short packet for each line 1: Send line short packet for each line Bit[3:0]: Not used
0x4801	MIPI CTRL01	0x00	RW	Bit[7]: Not used Bit[6]: spkt_dt_sel 1: Use dt_spkt as short packet data Bit[5]: first_bit Change clk_lane first bit 0: Output 8'h5 1: Output 8'hAA Bit[4]: Reserved Bit[3:2]: Not used Bit[1]: LPX_select for pclk domain 0: Auto calculate t_lpx_p Unit pclk2x cycle 1: Use lpx_p_min[7:0] Bit[0]: Not used

table 6-22 MIPI control registers (sheet 2 of 14)

address	register name	default value	R/W	description
0x4802	MIPI CTRL02	0x00	RW	Bit[7]: hs_prepare_sel 0: Auto calculate T_hs_prepare, unit pclk2x 1: Use hs_prepare_min_o[7:0] Bit[6]: clk_prepare_sel 0: Auto calculate T_clk_prepare, unit pclk2x 1: Use clk_prepare_min_o[7:0] Bit[5]: clk_post_sel 0: Auto calculate T_clk_post, unit pclk2x 1: Use clk_post_min_o[7:0] Bit[4]: clk_trail_sel 0: Auto calculate T_clk_trail, unit pclk2x 1: Use clk_trail_min_o[7:0] Bit[3]: hs_exit_sel 0: Auto calculate T_hs_exit, unit pclk2x 1: Use hs_exit_min_o[7:0] Bit[2]: hs_zero_sel 0: Auto calculate T_hs_zero, unit pclk2x 1: Use hs_zero_min_o[7:0] Bit[1]: hs_trail_sel 0: Auto calculate T_hs_trail, unit pclk2x 1: Use hs_trail_min_o[7:0] Bit[0]: clk_zero_sel 0: Auto calculate T_clk_zero, unit pclk2x 1: Use clk_zero_min_o[7:0]
0x4803	MIPI CTRL03	0x00	RW	Bit[7:4]: Not used Bit[3]: manu_ofset_o t_perio manual offset SMIA Bit[2]: r_manu_half2one t_period half to 1 SMIA Bit[1]: clk_pre_half_o Bit[0]: hs_pre_half_o
0x4804	MIPI CTRL04	0x44	RW	Bit[7:4]: man_lane_num Bit[3]: lane_num_manual_enable Bit[2]: lane4_6b_en 1: Support 4, 7, 8-lane 6-bit Bit[1]: vsub_s_o Bit[0]: vfifo_8x_o

table 6-22 MIPI control registers (sheet 3 of 14)

address	register name	default value	R/W	description
0x4805	MIPI CTRL05	0x00	RW	Bit[7:4]: Not used Bit[3]: lpda_retim_manu_o Bit[2]: lpda_retim_sel_o 1: Manual Bit[1]: lpck_retim_manu_o Bit[0]: lpck_retim_sel_o 1: Manual
0x4806	MIPI CTRL06	0x00	RW	Bit[7:5]: Not used Bit[4]: pu_mark_en_o Power up mark1 enable Bit[3]: mipi_remot_rst Bit[2]: mipi_susp Bit[1]: smia_lane_ch_en Bit[0]: tx_lsb_first 0: High bit first 1: Low power tx low bit first
0x4807	MIPI CTRL07	0x03	RW	Bit[7:4]: Not used Bit[3:0]: sw_t_lpx ul_tx T_lpx
0x4808	MIPI CTRL08	0x18	RW	Bit[7:0]: wkup_dly Mark1 wakeup delay/2^10
0x4809	MIPI CTRL09	0x2B	RW	Bit[7:6]: Not used Bit[5:0]: PDAF data type Manual data type
0x4810	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[15:8] High byte of max frame counter of frame sync short packet
0x4811	FCNT MAX	0xFF	RW	Bit[7:0]: fcnt_max[7:0] Low byte of max frame counter of frame sync short packet
0x4812	MIPI CTRL12	0x2B	RW	Bit[7:0]: dt_man2 Manual data type
0x4813	MIPI CTRL13	0x90	RW	Bit[7:6]: Virtual channel2 of MIPI Bit[5:4]: Virtual channel1 of MIPI Bit[3]: Not used Bit[2]: vc_sel Input VC or register VC Bit[1:0]: Virtual channel0 of MIPI
0x4814	MIPI CTRL14	0x2B	RW	Bit[7:0]: dt_man Manual data type

table 6-22 MIPI control registers (sheet 4 of 14)

address	register name	default value	R/W	description
0x4815	MIPI CTRL15	0x40	RW	Bit[7]: lpkt_dt_sel_o Bit[6]: pclk_inv 0: Using falling edge of mipi_pclk_o to generate MIPI bus to PHY 1: Using rising edge of mipi_pclk_o to generate MIPI bus to PHY Bit[5:0]: manu_dt_short Manual type for short packet
0x4816	EMB DT	0x52	RW	Bit[7]: Not used Bit[6]: Reserved Bit[5:0]: emb_dt Manually set embedded data type
0x4817	YUV	0x00	RW	Bit[7:3]: Not used Bit[2]: r_crc_1d Bit[1]: yuv420_en Bit[0]: yuv420_2x
0x4818	HS ZERO MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_zero_min[9:8] High byte of minimum value of hs_zero, unit ns
0x4819	HS ZERO MIN	0x70	RW	Bit[7:0]: hs_zero_min[7:0] Low byte of minimum value of hs_zero, unit ns hs_zero_real = hs_zero_min_o + Tui*ui_hs_zero_min_o
0x481A	HS TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_trail_min[9:8] High byte of minimum value of hs_trail, unit ns
0x481B	HS TRAIL MIN	0x3C	RW	Bit[7:0]: hs_trail_min[7:0] Low byte of minimum value of hs_trail, unit ns hs_trail_real = hs_trail_min_o + Tui*ui_hs_trail_min_o
0x481C	CLK ZERO MIN	0x01	RW	Bit[7:2]: Not used Bit[1:0]: clk_zero_min[9:8] High byte of minimum value of clk_zero, unit ns
0x481D	CLK ZERO MIN	0x2C	RW	Bit[7:0]: clk_zero_min[7:0] Low byte of minimum value of clk_zero, unit ns clk_zero_real = clk_zero_min_o + Tui*ui_clk_zero_min_o

table 6-22 MIPI control registers (sheet 5 of 14)

address	register name	default value	R/W	description
0x481E	CLK PREPARE MAX	0x5F	RW	Bit[7:0]: clk_prepare_max[7:0] Maximum value of clk_prepare, unit ns
0x481F	CLK PREPARE MIN	0x26	RW	Bit[7:0]: clk_prepare_min[7:0] Minimum value of clk_prepare clk_prepare_real = clk_prepare_min_o + Tui*ui_clk_prepare_min_o
0x4820	CLK POST MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_post_min[9:8] High byte of minimum value of clk_post, unit ns
0x4821	CLK POST MIN	0x3C	RW	Bit[7:0]: clk_post_min[7:0] Low byte of minimum value of clk_post, unit ns clk_post_real = clk_post_min_o + Tui*ui_clk_post_min_o
0x4822	CLK TRAIL MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: clk_trail_min[9:8] High byte of minimum value of clk_trail, unit ns
0x4823	CLK TRAIL MIN	0x3C	RW	Bit[7:0]: clk_trail_min[7:0] Low byte of minimum value of clk_trail, unit ns clk_trail_real = clk_trail_min_o + Tui*ui_clk_trail_min_o
0x4824	LPX P MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: lpx_p_min[9:8] High byte of minimum value of lpx_p, unit ns
0x4825	LPX P MIN	0x32	RW	Bit[7:0]: lpx_p_min[7:0] Low byte of minimum value of lpx_p, unit ns lpx_p_real = lpx_p_min_o + Tui*ui_lpx_p_min_o
0x4826	HS PREPARE MIN	0x32	RW	Bit[7:0]: hs_prepare_min[7:0] Minimum value of hs_prepare, unit ns
0x4827	HS PREPARE MAX	0x55	RW	Bit[7:0]: hs_prepare_max[7:0] Maximum value of hs_prepare hs_prepare_real = hs_prepare_max_o + Tui*ui_hs_prepare_max_o

table 6-22 MIPI control registers (sheet 6 of 14)

address	register name	default value	R/W	description
0x4828	HS EXIT MIN	0x00	RW	Bit[7:2]: Not used Bit[1:0]: hs_exit_min[9:8] High byte of minimum value of hs_exit, unit ns
0x4829	HS EXIT MIN	0x64	RW	Bit[7:0]: hs_exit_min[7:0] Low byte of minimum value of hs_exit, unit ns hs_exit_real = hs_exit_min_o + Tui*ui_hs_exit_min_o
0x482A	UI HS ZERO MIN	0x06	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_zero_min[5:0] Minimum UI value of hs_zero, unit UI
0x482B	UI HS TRAIL MIN	0x04	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_trail_min[5:0] Minimum UI value of hs_trail, unit UI
0x482C	UI CLK ZERO MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_zero_min[5:0] Minimum UI value of clk_zero, unit UI
0x482D	UI CLK PREPARE	0x00	RW	Bit[7:4]: ui_clk_prepare_max Maximum UI value of clk_prepare, unit UI Bit[3:0]: ui_clk_prepare_min Minimum UI value of clk_prepare, unit UI
0x482E	UI CLK POST MIN	0x34	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_post_min[5:0] Minimum UI value of clk_post, unit UI
0x482F	UI CLK TRAIL MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_clk_trail_min[5:0] Minimum UI value of clk_trail, unit UI
0x4830	UI LPX P MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_lpx_p_min[5:0] Minimum UI value of lpx_p(pclk2x domain), unit UI
0x4831	UI HS PREPARE	0x64	RW	Bit[7:4]: ui_hs_prepare_max Maximum UI value of hs_prepare, unit UI Bit[3:0]: ui_hs_prepare_min Minimum UI value of hs_prepare, unit UI

table 6-22 MIPI control registers (sheet 7 of 14)

address	register name	default value	R/W	description
0x4832	UI HS EXIT MIN	0x00	RW	Bit[7:6]: Not used Bit[5:0]: ui_hs_exit_min[5:0] Minimum UI value of hs_exit, unit UI
0x4833	MIPI PKT STAR SIZE	0x18	RW	Bit[7:6]: Not used Bit[5:0]: rdy_mark_o
0x4834~ 0x4835	RSVD	–	–	Reserved
0x4836	GLB MODE SEL	0x00	RW	Bit[7:1]: Not used Bit[0]: smia_cal_en 0: Use period to calculate 1: Use SMIA bitrate to calculate
0x4837	PCLK PERIOD	0x08	RW	Bit[7:0]: pclk_period[7:0] Period of pclk2x, pclk_div=1, and 1 bit decimal
0x4838	MIPI LP GPIO0	0x00	RW	Bit[7]: lp_sel0 0: Auto generate mipi_lp_dir0_o 1: Use lp_dir_man0 to be mipi_lp_dir0_o Bit[6]: lp_dir_man0 0: Input 1: Output Bit[5]: lp_p0_o Bit[4]: lp_n0_o Bit[3]: lp_sel1 0: Auto generate mipi_lp_dir1_o 1: Use lp_dir_man1 to be mipi_lp_dir1_o Bit[2]: lp_dir_man1 0: Input 1: Output Bit[1]: lp_p1_o Bit[0]: lp_n1_o

table 6-22 MIPI control registers (sheet 8 of 14)

address	register name	default value	R/W	description
0x4839	MIPI LP GPIO1	0x00	RW	Bit[7]: lp_sel2 0: Auto generate mipi_lp_dir2_o 1: Use lp_dir_man2 to be mipi_lp_dir2_o Bit[6]: lp_dir_man2 0: Input 1: Output Bit[5]: lp_p2_o Bit[4]: lp_n2_o Bit[3]: lp_sel3 0: Auto generate mipi_lp_dir3_o 1: Use lp_dir_man3 to be mipi_lp_dir3_o Bit[2]: lp_dir_man3 0: Input 1: Output Bit[1]: lp_p3_o Bit[0]: lp_n3_o
0x483A	MIPI LP GPIO2	0x00	RW	Bit[7]: lp_sel4 0: Auto generate mipi_lp_dir4_o 1: Use lp_dir_man4 to be mipi_lp_dir4_o Bit[6]: lp_dir_man4 0: Input 1: Output Bit[5]: lp_p4_o Bit[4]: lp_n4_o Bit[3]: lp_sel5 0: Auto generate mipi_lp_dir5_o 1: Use lp_dir_man5 to be mipi_lp_dir5_o Bit[2]: lp_dir_man5 0: Input 1: Output Bit[1]: lp_p5_o Bit[0]: lp_n5_o

table 6-22 MIPI control registers (sheet 9 of 14)

address	register name	default value	R/W	description
0x483B	MIPI LP GPIO3	0x00	RW	Bit[7]: lp_sel6 0: Auto generate mipi_lp_dir6_o 1: Use lp_dir_man6 to be mipi_lp_dir6_o Bit[6]: lp_dir_man6 0: Input 1: Output Bit[5]: lp_p6_o Bit[4]: lp_n6_o Bit[3]: lp_sel7 0: Auto generate mipi_lp_dir7_o 1: Use lp_dir_man7 to be mipi_lp_dir7_o Bit[2]: lp_dir_man7 0: Input 1: Output Bit[1]: lp_p7_o Bit[0]: lp_n7_o
0x483C	MIPI CTRL3C	0x02	RW	Bit[7:4]: Not used Bit[3:0]: t_clk_pre Unit pclk2x cycle
0x483D	MIPI LP GPIO4	0x00	RW	Bit[7]: lp_ck_sel0 0: Auto generate mipi_ck_lp_dir0_o 1: Use lp_ck_dir_man0 to be mipi_ck_lp_dir0_o Bit[6]: lp_ck_dir_man0 0: Input 1: Output Bit[5]: lp_ck_p0_o Bit[4]: lp_ck_n0_o Bit[3]: lp_ck_sel1 0: Auto generate mipi_ck_lp_dir1_o 1: Use lp_ck_dir_man1 to be mipi_ck_lp_dir1_o Bit[2]: lp_ck_dir_man1 0: Input 1: Output Bit[1]: lp_ck_p1_o Bit[0]: lp_ck_n1_o
0x483E~ 0x4849	RSVD	–	–	Reserved

table 6-22 MIPI control registers (sheet 10 of 14)

address	register name	default value	R/W	description
0x484A	SEL MIPI CTRL4A	0x3F	RW	Bit[7:6]: Not used Bit[5]: slp_lp_pon_man_o Set for power up Bit[4]: slp_lp_pon_da Bit[3]: slp_lp_pon_ck Bit[2]: mipi_slp_man_st MIPI bus status manual control enable in sleep mode Bit[1]: clk_lane_state Bit[0]: data_lane_state
0x484B	SMIA OPTION	0x01	RW	Bit[7:4]: Not used Bit[3]: same_skew_o Bit[2]: line_st_sel_o 0: Line starts after HREF 1: Line starts after fifo_st Bit[1]: clk_start_sel_o 0: Clock starts after SOF 1: Clock starts after reset Bit[0]: sof_sel_o 0: Frame starts after HREF starts 1: Frame starts after SOF
0x484C	SEL MIPI CTRL4C	0x03	RW	Bit[7]: Not used Bit[6]: smia_fcnt_i select Bit[5]: prbs_enable Bit[4]: hs_test_only MIPI high speed only test mode enable Bit[3]: set_frame_cnt_0 Set frame count to inactive mode (keep 0) Bit[2:0]: Not used
0x484D	TEST PATTEN DATA	0xB6	RW	Bit[7:0]: test_patten_data[7:0] Data lane test pattern register
0x484E	FE DLY	0x10	RW	Bit[7:0]: r_fe_dly_o Last packet to frame end delay / 2
0x484F	TEST PATTEN CK DATA	0x55	RW	Bit[7:0]: clk_test_patten_reg
0x4850	R DE SKEW	0x7C	RW	Bit[7:2]: r_de_skew_dly Bit[1]: r_de_skew_manu1 Bit[0]: r_de_skew_manu0
0x4851	R SKEW COMMOND	0x01	RW	Bit[7:0]: r_skew_commond
0x4852	R DE SKEW DLY	0x06	RW	Bit[7:0]: r_de_skew_dly
0x4853	R SW RDY	0x28	R	Bit[7:0]: init_dskew_dly

table 6-22 MIPI control registers (sheet 11 of 14)

address	register name	default value	R/W	description
0x4854	R SKEW CNT START0	0x3E	RW	Bit[7:0]: r_skew_cnt_start0
0x4855	R SKEW CNT START1 L	0x90	RW	Bit[7:0]: r_skew_cnt_start1[7:0]
0x4856	R MODE	0x58	RW	Bit[7:6]: Not used Bit[5]: deskew_out_en Bit[4]: r_skew_cnt_start1[8] Bit[3]: r_trail_same_start Bit[2]: r_mode12_tradat Bit[1:0]: r_mode
0x4857	R MODE12 HSDAT	0xAA	RW	Bit[7:0]: r_mode12_hsdat
0x4858	R MODE2 SYNCDAT1	0xFF	RW	Bit[7:0]: r_mode2_syncdat1
0x4859	R MODE2 SYNCDAT2	0xFF	RW	Bit[7:0]: r_mode2_syncdat2
0x485A	R MODE3 PREADAT1	0xFF	RW	Bit[7:0]: r_mode3_preadat1
0x485B	R MODE3 PREADAT2	0x3F	RW	Bit[7:0]: r_mode3_preadat2
0x485C	R MODE3 PREADAT SEL	0x2A	RW	Bit[7:0]: r_mode3_preadat_sel
0x485D	R PROGDAT1	0x66	RW	Bit[7:0]: r_progdat1
0x485E	R PROGDAT2	0x99	RW	Bit[7:0]: r_progdat2
0x485F	R PROGDAT3	0x88	RW	Bit[7:0]: r_progdat3
0x4860	R PROGDAT4	0xAA	RW	Bit[7:0]: r_progdat4
0x4861	R MODE3 PROGDAT SEL L	0xAA	RW	Bit[7:0]: r_mode3_progdat_sel[7:0]
0x4862	R MODE3 PROGDAT SEL H	0x0A	RW	Bit[7:0]: r_mode3_progdat_sel[15:8]
0x4863	R MODE3 SYNCDAT1	0x84	RW	Bit[7:0]: r_mode3_syncdat1
0x4864	R MODE3 SYNCDAT2	0x36	RW	Bit[7:0]: r_mode3_syncdat2
0x4865	R MODE3 SYNCDAT SEL	0x2A	RW	Bit[7:0]: r_mode3_syncdat_sel
0x4866	TPREBEGIN	0x01	RW	Bit[7:0]: Tprebegin
0x4867	TPROGSEQ	0x02	RW	Bit[7:0]: Tprogseq
0x4868	TPREEND	0x01	RW	Bit[7:0]: Tpreend

table 6-22 MIPI control registers (sheet 12 of 14)

address	register name	default value	R/W	description
0x4869	MODE3 CTR	0x18	RW	Bit[7:5]: Not used Bit[4]: Mode3 phorder select Bit[3]: eot_same Bit[2]: crc_mode3_sel Bit[1]: mode3_tradat Bit[0]: mode3_trail_man
0x486A	R MODE3 PH SEL	0xAA	RW	Bit[7:0]: r_mode3_ph_sel
0x486B	R MODE3 RESERDAT	0x00	RW	Bit[7:0]: r_mode3_reserdat
0x486C	R MODE3 ESC DAT1	0x84	RW	Bit[7:0]: r_mode3_esc_dat1
0x486D	R MODE3 ESC DAT2	0x36	RW	Bit[7:0]: r_mode3_esc_dat2
0x486E	MIPI CTRL6E	0x03	RW	Bit[7:4]: Not used Bit[3]: Data type enable Bit[2]: Virtual channel enable Bit[1]: clk_trail_data Bit[0]: mode3_cphy
0x486F	R MODE12 CLK DATA	0x55	RW	Bit[7:0]: r_mode12_clk_data
0x4870	MIPI CTRL70	0x48	RW	Bit[7]: Not used Bit[6]: r_skew_man_sel Bit[5:3]: r_lane1_swap Bit[2:0]: r_lane0_swap
0x4871	MIPI CTRL71	0x1A	RW	Bit[7:6]: Not used Bit[5:3]: r_lane3_swap Bit[2:0]: r_lane2_swap
0x4872	MIPI CTRL72	0x2C	RW	Bit[7]: r_slp_change_en Bit[6]: r_pkt_slp_en Bit[5:3]: r_lane5_swap Bit[2:0]: r_lane4_swap
0x4873	MIPI CTRL73	0x12	RW	Bit[7:4]: Not used Bit[3]: r_clk_start_early Bit[2:0]: r_mode2_sync_cnt
0x4874	R MODE2 SYNCDAT3	0xFF	RW	Bit[7:0]: r_mode2_syncdat3
0x4875	R LANE1 START	0xF0	RW	Bit[7:0]: r_lane1_start
0x4876	R CPHY MANUAL	0x08	RW	Bit[7:0]: r_cphy_manual
0x4877	R DUMMY DATA15	0x00	RW	Bit[7:0]: r_dummy_data15
0x4878	R DUMMY DATA14	0x00	RW	Bit[7:0]: r_dummy_data14
0x4879	R DUMMY DATA13	0xE7	RW	Bit[7:0]: r_dummy_data13
0x487A	R DUMMY DATA12	0x24	RW	Bit[7:0]: r_dummy_data12
0x487B	R DUMMY DATA11	0x01	RW	Bit[7:0]: r_dummy_data11

table 6-22 MIPI control registers (sheet 13 of 14)

address	register name	default value	R/W	description
0x487C	R DUMMY DATA10	0x00	RW	Bit[7:0]: r_dummy_data10
0x487D	R DUMMY DATA9	0x34	RW	Bit[7:0]: r_dummy_data9
0x487E	R DUMMY DATA8	0x00	RW	Bit[7:0]: r_dummy_data8
0x487F	R DUMMY DATA7	0x84	RW	Bit[7:0]: r_dummy_data7
0x4880	R DUMMY DATA6	0x36	RW	Bit[7:0]: r_dummy_data6
0x4881	R DUMMY DATA5	0x00	RW	Bit[7:0]: r_dummy_data5
0x4882	R DUMMY DATA4	0x00	RW	Bit[7:0]: r_dummy_data4
0x4883	R DUMMY DATA3	0xE7	RW	Bit[7:0]: r_dummy_data3
0x4884	R DUMMY DATA2	0x24	RW	Bit[7:0]: r_dummy_data2
0x4885	R DUMMY DATA1	0x01	RW	Bit[7:0]: r_dummy_data1
0x4886	R DUMMY DATA0	0x00	RW	Bit[7:0]: r_dummy_data0
0x4887	R MODE3 PROGDAT5	0x00	RW	Bit[7:0]: r_mode3_progdat5
0x4888	R MODE3 PROGDAT6	0x00	RW	Bit[7:0]: r_mode3_progdat6
0x4889	R MODE3 PROGDAT7	0x55	RW	Bit[7:0]: r_mode3_progdat7
0x488A	R MODE3 PROGDAT8	0x15	RW	Bit[7:0]: r_mode3_progdat8
0x488B	R MODE3 PROGDAT9	0xAA	RW	Bit[7:0]: r_mode3_progdat9
0x488C	R MODE3 PROGDAT10	0x2A	RW	Bit[7:0]: r_mode3_progdat10
0x488D	R MODE3 PROGDAT11	0xFF	RW	Bit[7:0]: r_mode3_progdat11
0x488E	R MODE3 PROGDAT12	0x3F	RW	Bit[7:0]: r_mode3_progdat12
0x488F	R MODE3 PROGDAT13	0x00	RW	Bit[7:0]: r_mode3_progdat13
0x4890	R MODE3 PROGDAT14	0x00	RW	Bit[7:0]: r_mode3_progdat14
0x4891	R MODE3 PROGDAT15	0x55	RW	Bit[7:0]: r_mode3_progdat15
0x4892	R MODE3 PROGDAT16	0x15	RW	Bit[7:0]: r_mode3_progdat16
0x4893	R MODE3 PROGDAT17	0xAA	RW	Bit[7:0]: r_mode3_progdat17

table 6-22 MIPI control registers (sheet 14 of 14)

address	register name	default value	R/W	description
0x4894	R MODE3 PROGDAT18	0x2A	RW	Bit[7:0]: r_mode3_progdat18
0x4895	R MODE3 PROGDAT19	0xFF	RW	Bit[7:0]: r_mode3_progdat19
0x4896	R MODE3 PROGDAT20	0x3F	RW	Bit[7:0]: r_mode3_progdat20
0x4897	R MODE3 PROGDAT21	0x00	RW	Bit[7:0]: r_mode3_progdat21
0x4898	R MODE3 PROGDAT22	0x00	RW	Bit[7:0]: r_mode3_progdat22
0x4899	R MODE3 PROGDAT23	0x55	RW	Bit[7:0]: r_mode3_progdat23
0x489A	R MODE3 PROGDAT24	0x15	RW	Bit[7:0]: r_mode3_progdat24
0x489B	R MODE3 PROGDAT25	0xAA	RW	Bit[7:0]: r_mode3_progdat25
0x489C	R MODE3 PROGDAT26	0x2A	RW	Bit[7:0]: r_mode3_progdat26
0x489D	R MODE3 PROGDAT27	0xFF	RW	Bit[7:0]: r_mode3_progdat27
0x489E	R MODE3 PROGDAT28	0x3F	RW	Bit[7:0]: r_mode3_progdat28
0x489F	R MODE2 SYNCDAT4	0xFF	RW	Bit[7:0]: r_mode2_syncdat4
0x48A0	R MODE2 SYNCDAT5	0xFF	RW	Bit[7:0]: r_mode2_syncdat5
0x48A1	R MODE2 SYNCDAT6	0xFF	RW	Bit[7:0]: r_mode2_syncdat6
0x48B6	PRBS_CTRL0	0x00	RW	Bit[7:0]: prbs_ctrl0
0x48B7	PRBS_CTRL1	0xFF	RW	Bit[7:0]: prbs_ctrl1
0x48B8	PRBS_CTRL2	0xFF	RW	Bit[7:0]: prbs_ctrl2
0x48B9	PRBS_CTRL3	0xFF	RW	Bit[7:0]: prbs_ctrl3
0x48BA	PRBS_CTRL4	0x00	RW	Bit[7:0]: prbs_ctrl4

6.23 temperature sensor [0x4D00 - 0x4D14]

table 6-23 temperature sensor registers

address	register name	default value	R/W	description
0x4D00~ 0x4D0F	TPM_CTRL_REG	–	–	Temperature Sensor Control Registers
0x4D10	TPM_CTRL_10	0x00	RW	Bit[7:0]: r_tpm_min
0x4D11	TPM_CTRL_11	0xFF	RW	Bit[7:0]: r_tpm_max
0x4D12	TPM_CTRL_12	–	W	Writing 0x4D12[0] to '1' will trigger temperature calculation, then registers 0x4D12 and 0x4D13 will be the latched temperature value
0x4D13	TPM_CTRL_13	–	R	Latched Temperature Value, Integer Part
0x4D14	TPM_CTRL_14	–	R	Latched Temperature Value, Decimal Part

6.24 AFC statistics control [0x4F00 - 0x4F24, 0x4F30 - 0x4F89, 0x4F8F]

table 6-24 AFC statistics control registers (sheet 1 of 6)

address	register name	default value	R/W	description
0x4F00	R AFC CTRL00	0x1C	RW	Bit[7]: lfhardthrehold Bit[6]: lfcenterhighpass Bit[5]: split_hdr3d_mode Bit[4]: rgbc_bin_order Bit[3]: channel_select Bit[2]: if_pro_scan Bit[1]: afc_mode Bit[0]: thre_man_en
0x4F01	R AFC CTRL01	0x04	RW	Bit[7:0]: contrast_scale
0x4F02	THRE MAN	0x00	RW	Bit[7:3]: Not used Bit[2:0]: thre_man[10:8]
0x4F03	THRE MAN	0x50	RW	Bit[7:0]: thre_man[7:0]
0x4F04	WIN X0	0x01	RW	Bit[7:5]: Not used Bit[4:0]: win_x0[12:8]
0x4F05	WIN X0	0x7C	RW	Bit[7:0]: win_x0[7:0]
0x4F06	WIN Y0	0x00	RW	Bit[7:4]: Not used Bit[3:0]: win_y0[11:8]

table 6-24 AFC statistics control registers (sheet 2 of 6)

address	register name	default value	R/W	description
0x4F07	WIN Y0	0x00	RW	Bit[7:0]: win_y0[7:0]
0x4F08	WIN W0	0x00	RW	Bit[7:3]: Not used Bit[2:0]: win_w0[10:8]
0x4F09	WIN W0	0x60	RW	Bit[7:0]: win_w0[7:0]
0x4F0A	WIN H0	0x00	RW	Bit[7:3]: Not used Bit[2:0]: win_h0[10:8]
0x4F0B	WIN H0	0x30	RW	Bit[7:0]: win_h0[7:0]
0x4F0C	WIN W1	0x01	RW	Bit[7:3]: Not used Bit[2:0]: win_w1[10:8]
0x4F0D	WIN W1	0xB8	RW	Bit[7:0]: win_w1[7:0]
0x4F0E	WIN H1	0x00	RW	Bit[7:3]: Not used Bit[2:0]: win_h1[10:8]
0x4F0F	WIN H	0xDC	RW	Bit[7:0]: win_h1[7:0]
0x4F10	WIN ID	0x0C	RW	Bit[7:0]: active_win_id
0x4F11	R AFC CTRL11	0x08	RW	Bit[7:0]: min_hf_num
0x4F12	SAT THRE	0x00	RW	Bit[7:4]: Not used Bit[3:0]: sat_thre[11:8]
0x4F13	SAT THRE	0xF0	RW	Bit[7:0]: sat_thre[7:0]
0x4F14	FILTER5 COEF0	0xF0	RW	Bit[7:0]: filter5_coef0[7:0]
0x4F15	FILTER5 COEF1	0xF0	RW	Bit[7:0]: filter5_coef1[7:0]
0x4F16	FILTER5 COEF2	0xF0	RW	Bit[7:0]: filter5_coef2[7:0]
0x4F17	FILTER5 COEF3	0xF0	RW	Bit[7:0]: filter5_coef3[7:0]
0x4F18	FILTER5 COEF4	0xF0	RW	Bit[7:0]: filter5_coef4[7:0]
0x4F19	FILTER5 WEIGHTVALUE	0x00	RW	Bit[7:5]: Not used Bit[4:0]: filter5_weightvalue[4:0]
0x4F1A	FILTER5 LIGHTWEIGHT	0x00	RW	Bit[7:0]: filter5_lightweight
0x4F1B	R AFC CTRL1B	0xC0	RW	Bit[7:6]: Not used Bit[5:0]: cfa_pattern
0x4F1C	R AFC CTRL1C	0x00	RW	Bit[7]: Not used Bit[6]: r_afc_sram_disable Bit[5]: r_afc_buf_test0 Bit[4]: r_afc_buf_rme0 Bit[3:0]: r_afc_buf_rm0

table 6-24 AFC statistics control registers (sheet 3 of 6)

address	register name	default value	R/W	description
0x4F1D	R AFC CTRL1D	0x00	RW	Bit[7]: Not used Bit[6]: r_sram_wemb_sel Bit[5]: r_afc_buf_test1 Bit[4]: r_afc_buf_rme1 Bit[3:0]: r_afc_buf_rm1
0x4F1E	R AFC CTRL1E	0x00	RW	Bit[7:6]: Not used Bit[5]: r_afc_buf_test2 Bit[4]: r_afc_buf_rme2 Bit[3:0]: r_afc_buf_rm2
0x4F1F	RSVD	–	–	Reserved
0x4F20	CTRL20	0x07	RW	Bit[7:5]: Not used Bit[4:0]: r_win_x_st_o[12:8]
0x4F21	CTRL21	0xD0	RW	Bit[7:0]: r_win_x_st_o[7:0]
0x4F22	CTRL22	0x03	RW	Bit[4:0]: r_win_size_o[12:8]
0x4F23	CTRL23	0x20	RW	Bit[7:0]: r_win_size_o[7:0]
0x4F24	R_SKIP_MODE_O	0x00	RW	Bit[7:6]: r_skip_mode_o Bit[5:0]: r_start_waittime_o
0x4F30	AFC_RO_CTRL30	–	R	Bit[7:3]: Reserved Bit[2:0]: ConstrastList_24[10:8]
0x4F31	AFC_RO_CTRL31	–	R	Bit[7:0]: ConstrastList_24[7:0]
0x4F32	AFC_RO_CTRL32	–	R	Bit[7:0]: HistogramHList_0
0x4F33	AFC_RO_CTRL33	–	R	Bit[7:0]: HistogramHList_1
0x4F34	AFC_RO_CTRL34	–	R	Bit[7:0]: HistogramHList_2
0x4F35	AFC_RO_CTRL35	–	R	Bit[7:0]: HistogramHList_3
0x4F36	AFC_RO_CTRL36	–	R	Bit[7:0]: HistogramHList_4
0x4F37	AFC_RO_CTRL37	–	R	Bit[7:0]: HistogramHList_5
0x4F38	AFC_RO_CTRL38	–	R	Bit[7:0]: HistogramHList_6
0x4F39	AFC_RO_CTRL39	–	R	Bit[7:0]: HistogramHList_7
0x4F3A	AFC_RO_CTRL3A	–	R	Bit[7:0]: HistogramHList_8
0x4F3B	AFC_RO_CTRL3B	–	R	Bit[7:0]: HistogramHList_9
0x4F3C	AFC_RO_CTRL3C	–	R	Bit[7:0]: HistogramHList_10
0x4F3D	AFC_RO_CTRL3D	–	R	Bit[7:0]: HistogramHList_11
0x4F3E	AFC_RO_CTRL3E	–	R	Bit[7:0]: HistogramHList_12
0x4F3F	AFC_RO_CTRL3F	–	R	Bit[7:0]: HistogramHList_13

table 6-24 AFC statistics control registers (sheet 4 of 6)

address	register name	default value	R/W	description
0x4F40	AFC_RO_CTRL40	–	R	Bit[7:0]: HistogramHList_14
0x4F41	AFC_RO_CTRL41	–	R	Bit[7:0]: HistogramHList_15
0x4F42	AFC_RO_CTRL42	–	R	Bit[7:0]: HistogramHList_16
0x4F43	AFC_RO_CTRL43	–	R	Bit[7:0]: HistogramHList_17
0x4F44	AFC_RO_CTRL44	–	R	Bit[7:0]: HistogramHList_18
0x4F45	AFC_RO_CTRL45	–	R	Bit[7:0]: HistogramHList_19
0x4F46	AFC_RO_CTRL46	–	R	Bit[7:0]: HistogramHList_20
0x4F47	AFC_RO_CTRL47	–	R	Bit[7:0]: HistogramHList_21
0x4F48	AFC_RO_CTRL48	–	R	Bit[7:0]: HistogramHList_22
0x4F49	AFC_RO_CTRL49	–	R	Bit[7:0]: HistogramHList_23
0x4F4A	AFC_RO_CTRL4A	–	R	Bit[7:0]: HistogramHList_24
0x4F4B	AFC_RO_CTRL4B	–	R	Bit[7:0]: HistogramHList_25
0x4F4C	AFC_RO_CTRL4C	–	R	Bit[7:0]: HistogramHList_26
0x4F4D	AFC_RO_CTRL4D	–	R	Bit[7:0]: HistogramHList_27
0x4F4E	AFC_RO_CTRL4E	–	R	Bit[7:0]: HistogramHList_28
0x4F4F	AFC_RO_CTRL4F	–	R	Bit[7:0]: HistogramHList_29
0x4F50	AFC_RO_CTRL50	–	R	Bit[7:0]: HistogramHList_30
0x4F51	AFC_RO_CTRL51	–	R	Bit[7:0]: HistogramHList_31
0x4F52	AFC_RO_CTRL52	–	R	Bit[7:0]: HistogramHList_32
0x4F53	AFC_RO_CTRL53	–	R	Bit[7:0]: HistogramHList_33
0x4F54	AFC_RO_CTRL54	–	R	Bit[7:0]: HistogramHList_34
0x4F55	AFC_RO_CTRL55	–	R	Bit[7:0]: HistogramHList_35
0x4F56	AFC_RO_CTRL56	–	R	Bit[7:0]: HistogramHList_36
0x4F57	AFC_RO_CTRL57	–	R	Bit[7:0]: HistogramHList_37
0x4F58	AFC_RO_CTRL58	–	R	Bit[7:0]: HistogramHList_38
0x4F59	AFC_RO_CTRL59	–	R	Bit[7:0]: HistogramHList_39
0x4F5A	AFC_RO_CTRL5A	–	R	Bit[7:0]: HistogramHList_40
0x4F5B	AFC_RO_CTRL5B	–	R	Bit[7:0]: HistogramHList_41
0x4F5C	AFC_RO_CTRL5C	–	R	Bit[7:0]: HistogramVList_0
0x4F5D	AFC_RO_CTRL5D	–	R	Bit[7:0]: HistogramVList_1

table 6-24 AFC statistics control registers (sheet 5 of 6)

address	register name	default value	R/W	description
0x4F5E	AFC_RO_CTRL5E	–	R	Bit[7:0]: HistogramVList_2
0x4F5F	AFC_RO_CTRL5F	–	R	Bit[7:0]: HistogramVList_3
0x4F60	AFC_RO_CTRL60	–	R	Bit[7:0]: HistogramVList_4
0x4F61	AFC_RO_CTRL61	–	R	Bit[7:0]: HistogramVList_5
0x4F62	AFC_RO_CTRL62	–	R	Bit[7:0]: HistogramVList_6
0x4F63	AFC_RO_CTRL63	–	R	Bit[7:0]: HistogramVList_7
0x4F64	AFC_RO_CTRL64	–	R	Bit[7:0]: HistogramVList_8
0x4F65	AFC_RO_CTRL65	–	R	Bit[7:0]: HistogramVList_9
0x4F66	AFC_RO_CTRL66	–	R	Bit[7:0]: HistogramVList_10
0x4F67	AFC_RO_CTRL67	–	R	Bit[7:0]: HistogramVList_11
0x4F68	AFC_RO_CTRL68	–	R	Bit[7:0]: HistogramVList_12
0x4F69	AFC_RO_CTRL69	–	R	Bit[7:0]: HistogramVList_13
0x4F6A	AFC_RO_CTRL6A	–	R	Bit[7:0]: HistogramVList_14
0x4F6B	AFC_RO_CTRL6B	–	R	Bit[7:0]: HistogramVList_15
0x4F6C	AFC_RO_CTRL6C	–	R	Bit[7:0]: HistogramVList_16
0x4F6D	AFC_RO_CTRL6D	–	R	Bit[7:0]: HistogramVList_17
0x4F6E	AFC_RO_CTRL6E	–	R	Bit[7:0]: HistogramVList_18
0x4F6F	AFC_RO_CTRL6F	–	R	Bit[7:0]: HistogramVList_19
0x4F70	AFC_RO_CTRL70	–	R	Bit[7:0]: HistogramVList_20
0x4F71	AFC_RO_CTRL71	–	R	Bit[7:0]: HistogramVList_21
0x4F72	AFC_RO_CTRL72	–	R	Bit[7:0]: HistogramVList_22
0x4F73	AFC_RO_CTRL73	–	R	Bit[7:0]: HistogramVList_23
0x4F74	AFC_RO_CTRL74	–	R	Bit[7:0]: HistogramVList_24
0x4F75	AFC_RO_CTRL75	–	R	Bit[7:0]: HistogramVList_25
0x4F76	AFC_RO_CTRL76	–	R	Bit[7:0]: HistogramVList_26
0x4F77	AFC_RO_CTRL77	–	R	Bit[7:0]: HistogramVList_27
0x4F78	AFC_RO_CTRL78	–	R	Bit[7:0]: HistogramVList_28
0x4F79	AFC_RO_CTRL79	–	R	Bit[7:0]: HistogramVList_29
0x4F7A	AFC_RO_CTRL7A	–	R	Bit[7:0]: HistogramVList_30
0x4F7B	AFC_RO_CTRL7B	–	R	Bit[7:0]: HistogramVList_31

table 6-24 AFC statistics control registers (sheet 6 of 6)

address	register name	default value	R/W	description
0x4F7C	AFC_RO_CTRL7C	–	R	Bit[7:0]: HistogramVList_32
0x4F7D	AFC_RO_CTRL7D	–	R	Bit[7:0]: HistogramVList_33
0x4F7E	AFC_RO_CTRL7E	–	R	Bit[7:0]: HistogramVList_34
0x4F7F	AFC_RO_CTRL7F	–	R	Bit[7:0]: HistogramVList_35
0x4F80	AFC_RO_CTRL80	–	R	Bit[7:0]: HistogramVList_36
0x4F81	AFC_RO_CTRL81	–	R	Bit[7:0]: HistogramVList_37
0x4F82	AFC_RO_CTRL82	–	R	Bit[7:0]: HistogramVList_38
0x4F83	AFC_RO_CTRL83	–	R	Bit[7:0]: HistogramVList_39
0x4F84	AFC_RO_CTRL84	–	R	Bit[7:0]: HistogramVList_40
0x4F85	AFC_RO_CTRL85	–	R	Bit[7:0]: HistogramVList_41
0x4F86	AFC_RO_CTRL86	–	R	Bit[7:6]: Reserved Bit[5:0]: HistogramHList length
0x4F87	AFC_RO_CTRL87	–	R	Bit[7:6]: Reserved Bit[5:0]: HistogramVList length
0x4F88	AFC_RO_CTRL88	–	R	Bit[7:0]: Saturate number[15:8]
0x4F89	AFC_RO_CTRL89	–	R	Bit[7:0]: Saturate number[7:0]
0x4F8F	AFC_RO_CTRL8F	–	R	Bit[7:2]: Not used Bit[1]: error_bit Bit[0]: afc_status_done

6.25 DSP control [0x5000 - 0x5079]

table 6-25 DSP control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x5000	R ISP CTRL00	0x8E	RW	Bit[7]: r_isp_en ISP enable Bit[6]: r_dcw_h_en DCW in horizontal direction enable Bit[5]: r_dcw_v_en DCW in vertical direction enable Bit[4]: r_vfpn_en VFPN cancellation enable Bit[3]: r_blc_en BLC enable Bit[2]: r_lenc_en LENC enable Bit[1]: r_awbg_en AWB gain enable Bit[0]: r_otp_en OTP data enable
0x5001	R ISP CTRL01	0xCB	RW	Bit[7]: r_swap_out_bypass Bit[6]: r_dpc_en DPC enable Bit[5]: Debug mode Bit[4]: Not used Bit[3]: r_pdf_en PD pixel remove enable Bit[2]: r_restore_pd_en Bit[1]: r_pdc_en Bit[0]: r_swap_in_bypass
0x5002	R ISP CTRL02	0x1C	RW	Bit[7:6]: Not used Bit[5:4]: Debug mode Bit[3:2]: Not used Bit[1]: r_vsync_pre_sel Bit[0]: r_vfpn_en1
0x5003	R ISP CTRL03	0x01	RW	Bit[7]: Not used Bit[6]: pre_dmy_count_en Bit[5:4]: Not used Bit[3]: r_isp_manu_ctrl_en Bit[2]: rgbc_en Bit[1]: r_sclk_global_en Bit[0]: Debug mode

table 6-25 DSP control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x5004	R ISP CTRL04	0x00	RW	Bit[7:6]: r_isp_sof_sel Bit[5:4]: r_expo_mode Exposure mode (works only when 0x5005[0] = 1) 00: Non-HDR 01: 2-exposure HDR 1x: Not allowed Bit[3:2]: r_hdr_ptn HDR pattern 00: Begin with long exposure 01: Begin with short exposure 10: Begin with very short exposure 11: Begin with medium exposure Bit[1:0]: r_cfa_ptn_man
0x5005	R ISP CTRL05	0x00	RW	Bit[7]: r_cfa_ptn_man_en Bit[6]: r_isp_mirror_man_en Bit[5]: r_isp_flip_man_en Bit[4]: r_blc_rblue_man_en Bit[3]: r_isp_blc_man_en Bit[2]: r_real_gain_man_en Bit[1]: r_insize_man_en Bit[0]: r_expo_mode_man_en Exposure manual mode enable 0: Auto mode 1: Manual mode
0x5006	R ISP CTRL06	0x00	RW	Bit[7:6]: Debug mode Bit[5]: r_scale_shift_man_en Scale ratio manual control enable Bit[4]: r_isp_flip_man Bit[3]: r_isp_mirror_man Bit[2]: gfirst_rvs Bit[1]: rblue_rvs Bit[0]: r_latch_en
0x5007~ 0x5008	DEBUG MODE	–	–	Debug Mode
0x5007	X_END_OFFSET	0x00	RW	X_end_offset
0x5008	Y_END_OFFSET	0x00	RW	Y_end_offset
0x5009	MAN ISP HSIZE	0x10	RW	Bit[7:5]: Not used Bit[4:0]: man_isp_hsize[12:8]
0x500A	MAN ISP HSIZE	0x80	RW	Bit[7:0]: man_isp_hsize[7:0]
0x500B	MAN ISP VSIZE	0x0C	RW	Bit[7:5]: Not used Bit[3:0]: man_isp_vsize[11:8]
0x500C	MAN ISP VSIZE	0x30	RW	Bit[7:0]: man_isp_vsize[7:0]

table 6-25 DSP control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x500D	MAN EXPO LONG REAL GAIN	0x00	RW	Bit[7:3]: Not used Bit[2:0]: man_expo_long_real_gain[10:8]
0x500E	MAN EXPO LONG REAL GAIN	0x10	RW	Bit[7:0]: man_expo_long_real_gain[7:0]
0x500F	MAN EXPO MEDIAN REAL GAIN	0x00	RW	Bit[7:3]: Not used Bit[2:0]: man_expo_median_real_gain[10:8]
0x5010	MAN EXPO MEDIAN REAL GAIN	0x10	RW	Bit[7:0]: man_expo_median_real_gain[7:0]
0x5011	MAN EXPO SHORT REAL GAIN	0x00	RW	Bit[7:3]: Not used Bit[2:0]: man_expo_short_real_gain[10:8]
0x5012	MAN EXPO SHORT REAL GAIN	0x10	RW	Bit[7:0]: man_expo_short_real_gain[7:0]
0x5013	MAN EXPO VSHORT REAL GAIN	0x00	RW	Bit[7:3]: Not used Bit[2:0]: man_expo_vshort_real_gain[10:8]
0x5014	MAN EXPO VSHORT REAL GAIN	0x10	RW	Bit[7:0]: man_expo_vshort_real_gain[7:0]
0x5015	MAN L BLC TARGET	0x00	RW	Bit[7:2]: Not used Bit[1:0]: man_l_blc_target[9:8]
0x5016	MAN L BLC TARGET	0x10	RW	Bit[7:0]: man_l_blc_target[7:0]
0x5017	MAN M BLC TARGET	0x00	RW	Bit[7:2]: Not used Bit[1:0]: man_m_blc_target[9:8]
0x5018	MAN M BLC TARGET	0x10	RW	Bit[7:0]: man_m_blc_target[7:0]
0x5019	MAN S BLC TARGET	0x00	RW	Bit[7:2]: Not used Bit[1:0]: man_s_blc_target[9:8]
0x501A	MAN S BLC TARGET	0x10	RW	Bit[7:0]: man_s_blc_target[7:0]
0x501B	MAN VS BLC TARGET	0x00	RW	Bit[7:2]: Not used Bit[1:0]: man_vs_blc_target[9:8]
0x501C	MAN VS BLC TARGET	0x10	RW	Bit[7:0]: man_vs_blc_target[7:0]

table 6-25 DSP control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x501D	R ISP CTRL1D	0x00	RW	Bit[7:6]: hscale_shift Manual value of horizontal down scale ratio (works only when register 0x5006[5] = 1) Bit[5:4]: vscale_shift Manual value of vertical down scale ratio (works only when register 0x5006[5] = 1) Bit[3]: r_blc_img_flg_en Bit[2]: blc_img_flg_inv Bit[1]: vfpn_hdr_mode_en Bit[0]: ls_order_flip_opt
0x501E	R ISP CTRL1E	0x3F	RW	Bit[7:4]: hdr_fmt Bit[3:0]: cen_vfpn
0x501F	R ISP CTRL1F	0x06	RW	Bit[7:6]: dig_gain_blc Bit[5:3]: r_win_y_offset_adjust Bit[2]: r_isp_raw_en Bit[1]: r_dcblc_en Bit[0]: r_cvdnblc_en
0x5020	R ISP CTRL20	0x03	RW	Bit[7]: r_zero_rblue_man_en Bit[6]: r_zero_rblue_man Bit[5]: r_blc_rblue_man Bit[4]: r_aec_stat_en Bit[3]: blc_vsync_sel Bit[2]: blc_px_man_en Bit[1]: vfpn_out_range_en Bit[0]: r_vfpn_sof_sel
0x5021	R ISP CTRL21	0x00	RW	Bit[7:6]: isp_bit_sel Bit[5:3]: r_eof_sel Bit[2:0]: r_out_fmt
0x5022	R ISP CTRL22	0x91	RW	Bit[7]: pdc_before_lenc_en Bit[6:5]: r_blc_ls_flag_sel Bit[4]: blc_ls_flag_long Bit[3:2]: blc_px_man Bit[1]: Debug mode Bit[0]: r_dpc_pad_en
0x5023~ 0x5056	DEBUG	–	–	Debug Mode
0x5057	R ISP CTRL57	0x00	RW	Bit[7]: r_dpc_sram_disable Bit[6:5]: Not used Bit[4]: r_full_buf_disable Bit[3]: r_vfpn_sram_disable Bit[2]: Debug mode Bit[1:0]: Not used

table 6-25 DSP control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x5058	R ISP CTRL58	0x00	RW	Bit[7:6]: Not used Bit[5]: r_bypass_lenc_pdc Bit[4]: Not used Bit[3:0]: Reserved
0x5059~ 0x505C	NOT USED	–	–	Not Used
0x505D	R ISP CTRL5D	0x00	RW	Bit[7]: r_isp_dly_num_manu_en Bit[6:0]: r_isp_dly_num_manu[14:8]
0x505E	R ISP DLY NUM MANU	0x40	RW	Bit[7:0]: r_isp_dly_num_manu[7:0]
0x505F	R ISP CLK DIS DLY	0x18	RW	Bit[7]: Not used Bit[6:0]: r_isp_clk_dis_dly[14:8]
0x5060	R ISP CLK DIS DLY	0x00	RW	Bit[7:0]: r_isp_clk_dis_dly[7:0]
0x5061	R ISP CTRL61	0x00	RW	Bit[7]: clk_gt_dis_isp Bit[6]: clk_gt_dis_dcw_h Bit[5]: clk_gt_dis_dcw_v Bit[4]: clk_gt_dis_vfpn Bit[3]: clk_gt_dis_blc Bit[2]: clk_gt_dis_lenc Bit[1]: clk_gt_dis_awbg Bit[0]: clk_gt_dis_otp
0x5062	R ISP CTRL62	0x08	RW	Bit[7]: clk_gt_dis_d2tod4 Bit[6]: clk_gt_dis_dpc Bit[5]: clk_gt_dis_d4_to_d2 Bit[4]: clk_gt_dis_var_pix Bit[3]: clk_gt_dis_vfpn1 Bit[2]: Not used Bit[1]: clk_gt_dis_restore_pd Bit[0]: clk_gt_dis_pdc
0x5063	R ISP CTRL63	0x00	RW	Bit[7:3]: Not used Bit[2:1]: Debug mode Bit[0]: clk_gt_dis_pdf
0x5064~ 0x5077	DEBUG	–	–	Debug Mode
0x5078	R PDC H SKIP	0x05	RW	Bit[7:0]: r_pdc_h_skip_o
0x5079	R PDC V SKIP	0x05	RW	Bit[7:0]: r_pdc_v_skip_o

6.26 MEC/MGC [0x3500 - 0x3521]

table 6-26 MEC/MGC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x3500	EXPO LONG PK	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Long exposure[19:16]
0x3501	MEC LONG EXPO	0x02	RW	Long Exposure Bit[7:0]: Long exposure[15:8]
0x3502	MEC LONG EXPO	0x00	RW	Long Exposure Bit[7:0]: Long exposure[7:0]
0x3503	R MANUAL	0x03	RW	Bit[7:6]: Not used Bit[5]: Gain delay option 0: 1 frame latch 1: Delay 1 frame latch Bit[4]: Choose delay option 0: Delay disable 1: Delay enable Bit[3]: Not used Bit[2]: vts_manual Bit[1]: agc_manual Bit[0]: aec_manual
0x3504	MAN GAIN SNR	0x00	RW	Bit[7:2]: Not used Bit[1:0]: man_gain_snr[9:8]
0x3505	MAN GAIN SNR	0x00	RW	Bit[7:0]: man_gain_snr[7:0]
0x3506	EXPO SHORT PK	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Short exposure[19:16]
0x3507	MEC SHORT EXPO	0x02	RW	Short Exposure Bit[7:0]: Short exposure[15:8]
0x3508	MEC SHORT EXPO	0x00	RW	Short Exposure Bit[7:0]: Short exposure[7:0]
0x3509	R CTRL9	0x12	RW	Bit[7:6]: Not used Bit[5]: gain_keep Bit[4]: convert_en Bit[3]: gain_man_en Bit[2]: expo_isp_sel Bit[1]: short_convert_en Bit[0]: short_gain_man_en
0x350A	MEC LONG GAIN	0x00	RW	Long Gain Bit[7:3]: Not used Bit[2:0]: Long gain[10:8]
0x350B	MEC LONG GAIN	0x10	RW	Long Gain Bit[7:0]: Long gain[7:0]

table 6-26 MEC/MGC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x350C	ADD VTS PK	0x00	RW	Bit[7:0]: add_vts_pk[15:8]
0x350D	ADD VTS PK	0x00	RW	Bit[7:0]: add_vts_pk[7:0]
0x350E	MEC SHORT GAIN	0x00	RW	Short Gain Bit[7:3]: Not used Bit[2:0]: Short gain[10:8]
0x350F	MEC SHORT GAIN	0x10	RW	Short Gain Bit[7:0]: Short gain[7:0]
0x3510	PK GAIN O	–	R	Bit[7:2]: Not used Bit[1:0]: pk_gain_o[9:8]
0x3511	PK GAIN O	–	R	Bit[7:0]: pk_gain_o[7:0]
0x3512	SNR GAIN	–	R	Bit[7:2]: Not used Bit[1:0]: snr_gain[9:8]
0x3513	SNR GAIN	–	R	Bit[7:0]: snr_gain[7:0]
0x3514	MAN SHORT GAIN SNR	0x00	RW	Bit[7:2]: Not used Bit[1:0]: man_short_gain_snr[9:8]
0x3515	MAN SHORT GAIN SNR	0x00	RW	Bit[7:0]: man_short_gain_snr[7:0]
0x3516	MAN LONG DGC	0x02	RW	Bit[7:2]: Not used Bit[1:0]: man_long_dgc[9:8]
0x3517	MAN LONG DGC	0x00	RW	Bit[7:0]: man_long_dgc[7:0]
0x3518	MAN SHORT DGC	0x02	RW	Bit[7:2]: Not used Bit[1:0]: man_short_dgc[9:8]
0x3519	MAN SHORT DGC	0x00	RW	Bit[7:0]: man_short_dgc[7:0]
0x351A	GAIN CALI Z0	0x00	RW	Bit[7:3]: Not used Bit[2:0]: gain_cali_z0[10:8]
0x351B	GAIN CALI Z0	0x10	RW	Bit[7:0]: gain_cali_z0[7:0]
0x351C	GAIN CALI Z0	0x00	RW	Bit[7:3]: Not used Bit[2:0]: gain_cali_z0[10:8]
0x351D	GAIN CALI Z0	0x20	RW	Bit[7:0]: gain_cali_z0[7:0]
0x351E	GAIN CALI Z0	0x00	RW	Bit[7:3]: Not used Bit[2:0]: gain_cali_z0[10:8]
0x351F	GAIN CALI Z0	0x40	RW	Bit[7:0]: gain_cali_z0[7:0]
0x3520	GAIN CALI Z0	0x00	RW	Bit[7:3]: Not used Bit[2:0]: gain_cali_z0[10:8]
0x3521	GAIN CALI Z0	0x80	RW	Bit[7:0]: gain_cali_z0[7:0]

6.27 pre_ISP [0x5280 - 0x5292, 0x52A0 - 0x52B4, 0x52B6 - 0x52B9]

table 6-27 pre_ISP registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5280	PRE CTRL00	0x00	RW	Bit[7]: Test pattern enable Bit[6]: Rolling bar function enable Bit[5]: Transparent enable 0: Disable transparent effect function 1: Enable transparent effect function Bit[4]: Square mode 0: Color square 1: Black-white square Bit[3:2]: Color bar style 00: Standard color bar 01: Top-bottom darker color bar 10: Right-left darker color bar 11: Bottom-top darker color bar Bit[1:0]: Test pattern mode 00: Color bar 01: Random data 10: Square pattern 11: Black image
0x5281	PRE CTRL01	0x01	RW	Bit[7]: Not used Bit[6]: Window cut enable 0: Do not cut the redundant pixels 1: Cut the redundant pixels Bit[5]: two_lsb_0_en When set, two LSBs of output data are 0 Bit[4]: Same seed enable When set, the seed used to generate the random data are same which is set in seed register Bit[3:0]: Random seed Seed used in generating random data
0x5282	LN INT	0x00	RW	Bit[7:5]: Not used Bit[4:0]: ln_int[12:8] Line number interrupt
0x5283	LN INT	0x01	RW	Bit[7:0]: ln_int[7:0] Line number interrupt
0x5284	SCALE X SIZE	0x00	RW	Bit[7:5]: Not used Bit[4:0]: scale_x_size[12:8] Scale X input manual size

table 6-27 pre_ISP registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5285	SCALE X SIZE	0x00	RW	Bit[7:0]: scale_x_size[7:0] Scale X input manual size
0x5286	SCALE Y SIZE	0x01	RW	Bit[7:4]: Not used Bit[3:0]: scale_y_size[11:8] Scale Y input manual size
0x5287	SCALE Y SIZE	0x00	RW	Bit[7:0]: scale_y_size[7:0] Scale Y input manual size
0x5288	X MANUAL OFFSET	0x00	RW	Bit[7:5]: Not used Bit[4:0]: x_manual_offset[12:8] X manual offset
0x5289	X MANUAL OFFSET	0x00	RW	Bit[7:0]: x_manual_offset[7:0] X manual offset
0x528A	Y MANUAL OFFSET	0x00	RW	Bit[7:4]: Not used Bit[3:0]: y_manual_offset[11:8] Y manual offset
0x528B	Y MANUAL OFFSET	0x00	RW	Bit[7:0]: y_manual_offset[7:0] Y manual offset
0x528C	PRE ISP CTRL16	0x30	RW	Bit[7:6]: Not used Bit[5]: Mirror option for X offset Bit[4]: Flip option for Y offset Bit[3]: Mirror order, BG or GB Bit[2]: Flip order, BR or RB Bit[1]: Offset manual enable 0: Disable 1: Enable Bit[0]: Scale input size manual mode 0: Disable 1: Enable
0x528D	PRE ISP CTRL17	0x00	RW	Bit[7]: Dummy line manual mode 0: Disable 1: Enable Bit[6:4]: Not used Bit[3]: Dummy line blanking half 0: Disable 1: Enable Bit[2:0]: Dummy line clock/data manual ratio
0x528E	LS RATIO	0x01	RW	Bit[7:0]: ls_ratio[15:8] Long/short ratio integer ratio part (short based mode) All 0 in HDR2 long based mode

table 6-27 pre_ISP registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x528F	LS RATIO	0x80	RW	Bit[7:0]: ls_ratio[7:0] Long/short ratio fraction part Short/long ratio in HDR2 long based mode
0x5290	MS RATIO	0x7F	RW	Bit[7:0]: ms_ratio[7:0] Middle/short ratio (HDR4 case)
0x5291	VS RATIO	0x3F	RW	Bit[7:0]: vs_ratio[7:0] Vshort/short ratio (HDR4 case)
0x5292	DUMMY LINE	0x00	RW	Bit[7:0]: dummy_line
0x52A0	DUMMY CNT HREF	–	R	Bit[7:0]: dummy_cnt_href[15:8] Dummy line clock number
0x52A1	DUMMY CNT HREF	–	R	Bit[7:0]: dummy_cnt_href[7:0] Dummy line clock number
0x52A2	DUMMY CNT BLANK	–	R	Bit[7:0]: dummy_cnt_blank[15:8] Dummy line blanking clock number
0x52A3	DUMMY CNT BLANK	–	R	Bit[7:0]: dummy_cnt_blank[7:0] Dummy line blanking clock number
0x52A4~ 0x52A5	NOT USED	–	–	Not Used
0x52A6	X OFFSET	–	R	Bit[7:5]: Not used Bit[4:0]: x_offset[12:8]
0x52A7	X OFFSET	–	R	Bit[7:0]: x_offset[7:0]
0x52A8	Y OFFSET	–	R	Bit[7:4]: Not used Bit[3:0]: y_offset[11:8]
0x52A9	Y OFFSET	–	R	Bit[7:0]: y_offset[7:0]
0x52AA	WIN X OFFSET	–	R	Bit[7:5]: Not used Bit[4:0]: win_x_offset[12:8]
0x52AB	WIN X OFFSET	–	R	Bit[7:0]: win_x_offset[7:0]
0x52AC	WIN Y OFFSET	–	R	Bit[7:4]: Not used Bit[3:0]: win_y_offset[11:8]
0x52AD	WIN Y OFFSET	–	R	Bit[7:0]: win_y_offset[7:0]
0x52AE	WIN Y OUTPUT	–	R	Bit[7:5]: Not used Bit[4:0]: win_y_output[12:8]
0x52AF	WIN X OUTPUT	–	R	Bit[7:0]: win_x_output[7:0]
0x52B0	WIN Y OUTPUT	–	R	Bit[7:4]: Not used Bit[3:0]: win_y_output[11:8]

table 6-27 pre_ISP registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x52B1	WIN Y OUTPUT	–	R	Bit[7:0]: win_y_output[7:0]
0x52B2	PRE ISP CTRL36	–	R	Bit[7:6]: Not used Bit[5:4]: X skip Bit[3:2]: Not used Bit[1:0]: Y skip
0x52B3	PRE ISP CTRL37	–	R	Bit[7:4]: X even inc[3:0] Horizontal skip Bit[3:0]: Y even inc[3:0] Vertical skip
0x52B4	PRE ISP CTRL38	–	R	Bit[7:4]: Not used Bit[3]: X odd inc[4] Bit[2]: Y odd inc[4] Bit[1]: X even inc[4] Bit[0]: Y even inc[4]
0x52B6	PX CNT	–	R	Bit[7:5]: Not used Bit[4:0]: px_cnt[12:8] Pixel number
0x52B7	PX CNT	–	R	Bit[7:0]: px_cnt[7:0] Pixel number
0x52B8	LN CNT	–	R	Bit[7:4]: Not used Bit[3:0]: ln_cnt[11:8] Line number
0x52B9	LN CNT	–	R	Bit[7:0]: ln_cnt[7:0] Line number

6.28 MWB gain control [0x5300 - 0x5316, 0x5320 - 0x5336, 0x5340 - 0x5383]

table 6-28 MWB gain control registers (sheet 1 of 5)

address	register name	default value	R/W	description
0x5300	R GAIN B L_H	0x04	RW	B Gain in Long Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_b_l[13:8]
0x5301	R GAIN B L_L	0x00	RW	B Gain in Long Exposure Bit[7:0]: r_gain_b_l[7:0]

table 6-28 MWB gain control registers (sheet 2 of 5)

address	register name	default value	R/W	description
0x5302	R GAIN GB L_H	0x04	RW	Gb Gain in Long Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_gb_l[13:8]
0x5303	R GAIN GB L_L	0x00	RW	Gb Gain in Long Exposure Bit[7:0]: r_gain_gb_l[7:0]
0x5304	R GAIN GR L_H	0x04	RW	Gr Gain in Long Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_gr_l[13:8]
0x5305	R GAIN GR L_L	0x00	RW	Gr Gain in Long Exposure Bit[7:0]: r_gain_gr_l[7:0]
0x5306	R GAIN R L_H	0x04	RW	R Gain in Long Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_r_l[13:8]
0x5307	R GAIN R L_L	0x00	RW	R Gain in Long Exposure Bit[7:0]: r_gain_r_l[7:0]
0x5308	R OFFSET B L_H	0x00	RW	B Offset in Long Exposure Bit[7:0]: r_offset_b_l[23:16]
0x5309	R OFFSET B L_M	0x00	RW	B Offset in Long Exposure Bit[7:0]: r_offset_b_l[15:8]
0x530A	R OFFSET B L_L	0x00	RW	B Offset in Long Exposure Bit[7:0]: r_offset_b_l[7:0]
0x530B	NOT USED	–	–	Not Used
0x530C	R OFFSET GB L_H	0x00	RW	Gb Offset in Long Exposure Bit[7:0]: r_offset_gb_l[23:16]
0x530D	R OFFSET GB L_M	0x00	RW	Gb Offset in Long Exposure Bit[7:0]: r_offset_gb_l[15:8]
0x530E	R OFFSET GB L_L	0x00	RW	Gb Offset in Long Exposure Bit[7:0]: r_offset_gb_l[7:0]
0x530F	NOT USED	–	–	Not Used
0x5310	R OFFSET GR L_H	0x00	RW	Gr Offset in Long Exposure Bit[7:0]: r_offset_gr_l[23:16]
0x5311	R OFFSET GR L_M	0x00	RW	Gr Offset in Long Exposure Bit[7:0]: r_offset_gr_l[15:8]
0x5312	R OFFSET GR L_L	0x00	RW	Gr Offset in Long Exposure Bit[7:0]: r_offset_gr_l[7:0]
0x5314	R OFFSET R L_H	0x00	RW	R Offset in Long Exposure Bit[7:0]: r_offset_r_l[23:16]

table 6-28 MWB gain control registers (sheet 3 of 5)

address	register name	default value	R/W	description
0x5315	R OFFSET R L_M	0x00	RW	R Offset in Long Exposure Bit[7:0]: r_offset_r_l[15:8]
0x5316	R OFFSET R L_L	0x00	RW	R Offset in Long Exposure Bit[7:0]: r_offset_r_l[7:0]
0x5320~ 0x5336	NOT USED	–	–	Not Used
0x5340	R GAIN B S_H	0x04	RW	B Gain in Short Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_b_s[13:8]
0x5341	R GAIN B S_L	0x00	RW	B Gain in Short Exposure Bit[7:0]: r_gain_b_s[7:0]
0x5342	R GAIN GB S_H	0x04	RW	Gb Gain in Short Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_gb_s[13:8]
0x5343	R GAIN GB S_L	0x00	RW	Gb Gain in Short Exposure Bit[7:0]: r_gain_gb_s[7:0]
0x5344	R GAIN GR S_H	0x04	RW	Gr Gain in Short Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_gr_s[13:8]
0x5345	R GAIN GR S_L	0x00	RW	Gr Gain in Short Exposure Bit[7:0]: r_gain_gr_s[7:0]
0x5346	R GAIN R S_H	0x04	RW	R Gain in Short Exposure Bit[7:6]: Not used Bit[5:0]: r_gain_r_s[13:8]
0x5347	R GAIN R S_L	0x00	RW	R Gain in Short Exposure Bit[7:0]: r_gain_r_s[7:0]
0x5348	R OFFSET B S_H	0x00	RW	B Offset in short Exposure Bit[7:0]: r_offset_b_s[23:16]
0x5349	R OFFSET B S_M	0x00	RW	B Offset in Short Exposure Bit[7:0]: r_offset_b_s[15:8]
0x534A	R OFFSET B S_L	0x00	RW	B Offset in Short Exposure Bit[7:0]: r_offset_b_s[7:0]
0x534B	NOT USED	–	–	Not Used
0x534C	R OFFSET GB S_H	0x00	RW	Gb Offset in Short Exposure Bit[7:0]: r_offset_gb_s[23:16]
0x534D	R OFFSET GB S_M	0x00	RW	Gb Offset in Short Exposure Bit[7:0]: r_offset_gb_s[15:8]

table 6-28 MWB gain control registers (sheet 4 of 5)

address	register name	default value	R/W	description
0x534E	R OFFSET GB S_L	0x00	RW	Gb Offset in Short Exposure Bit[7:0]: r_offset_gb_s[7:0]
0x534F	NOT USED	–	–	Not Used
0x5350	R OFFSET GR S_H	0x00	RW	Gr Offset in Short Exposure Bit[7:0]: r_offset_gr_s[23:16]
0x5351	R OFFSET GR S_M	0x00	RW	Gr Offset in Short Exposure Bit[7:0]: r_offset_gr_s[15:8]
0x5352	R OFFSET GR S_L	0x00	RW	Gr Offset in Short Exposure Bit[7:0]: r_offset_gr_s[7:0]
0x5353	NOT USED	–	–	Not Used
0x5354	R OFFSET R S_H	0x00	RW	R Offset in Short Exposure Bit[7:0]: r_offset_r_s[23:16]
0x5355	R OFFSET R S_M	0x00	RW	R Offset in Short Exposure Bit[7:0]: r_offset_r_s[15:8]
0x5356	R OFFSET R S_L	0x00	RW	R Offset in Short Exposure Bit[7:0]: r_offset_r_s[7:0]
0x5357~ 0x535F	RSVD	–	–	Reserved
0x5360~ 0x5376	NOT USED	–	–	Not Used
0x5377	R77	0x00	RW	Bit[7:3]: Not used Bit[2]: valid_latch_en Bit[1]: rgbc_ybin_en Bit[0]: rgbc_en
0x5378	RGBC BLC	0x00	RW	Bit[7:2]: Not used Bit[1:0]: rgbc_blc[9:8]
0x5379	RGBC BLC	0x00	RW	Bit[7:0]: rgbc_blc[7:0]
0x537A	RGBC GAIN B	0x04	RW	Bit[7:6]: Not used Bit[5:0]: rgbc_gain_b[13:8]
0x537B	RGBC GAIN B	0x00	RW	Bit[7:0]: rgbc_gain_b[7:0]
0x537C	RGBC GAIN GB	0x04	RW	Bit[7:6]: Not used Bit[5:0]: rgbc_gain_gb[13:8]
0x537D	RGBC GAIN GB	0x00	RW	Bit[7:0]: rgbc_gain_gb[7:0]
0x537E	RGBC GAIN GR	0x04	RW	Bit[7:6]: Not used Bit[5:0]: rgbc_gain_gr[13:8]
0x537F	RGBC GAIN GR	0x00	RW	Bit[7:0]: rgbc_gain_gr[7:0]

table 6-28 MWB gain control registers (sheet 5 of 5)

address	register name	default value	R/W	description
0x5380	RGBC GAIN R	0x04	RW	Bit[7:6]: Not used Bit[5:0]: rgbc_gain_r[13:8]
0x5381	RGBC GAIN R	0x00	RW	Bit[7:0]: rgbc_gain_r[7:0]
0x5382	RGBC GAIN C	0x04	RW	Bit[7:6]: Not used Bit[5:0]: rgbc_gain_c[13:8]
0x5383	RGBC GAIN C	0x00	RW	Bit[7:0]: rgbc_gain_c[7:0]

6.29 LENC control [0x2800 - 0x2B09, 0x2B10 - 0x2B16]

table 6-29 LENC control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x2800~ 0x28FF	COEFFICIENT FOR G CHANNEL	0x80	RW	Coefficient for G Channel
0x2900~ 0x29FF	COEFFICIENT FOR B CHANNEL	0x80	RW	Coefficient for B Channel
0x2A00~ 0x2AFF	COEFFICIENT FOR R CHANNEL	0x80	RW	Coefficient for R Channel
0x2B00	MAXGAIN	0x60	RW	Bit[7:0]: Maxgain[7:0]
0x2B01	MINGAIN	0x40	RW	Bit[7:0]: Mingain[7:0]
0x2B02	MAXQ	0x40	RW	Bit[7:0]: Maxq[7:0]
0x2B03	MINQ	0x18	RW	Bit[7:0]: Minq[7:0]
0x2B04	LENC CTRL0	0x36	RW	Bit[7:6]: Not used Bit[5]: Addblc Bit[4]: blc_en Bit[3]: Br2xmode Bit[2]: Lens correction control 0: Manually set Q value by register 0x2B02 1: Calculate Q according to real_gain Bit[1]: dither_en Bit[0]: g2xgain_en
0x2B05	HSCALE	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Hscale[12:8]
0x2B06	HSCALE	0xE1	RW	Bit[7:0]: Hscale[7:0]

table 6-29 LENC control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x2B07	VSCALE	0x01	RW	Bit[7:5]: Not used Bit[4:0]: Vscale[12:8]
0x2B08	VSCALE	0x41	RW	Bit[7:0]: Vscale[7:0]
0x2B09	R LENC CTRL1	0x00	RW	Bit[7:4]: Not used Bit[3:0]: dither_g[3:0]
0x2B10	X OFFSET	–	R	Bit[7:5]: Not used Bit[4:0]: x_offset[12:8]
0x2B11	X OFFSET	–	R	Bit[7:0]: x_offset[7:0]
0x2B12	Y OFFSET	–	R	Bit[7:5]: Not used Bit[4:0]: y_offset[12:8]
0x2B13	Y OFFSET	–	R	Bit[7:0]: y_offset[7:0]
0x2B14	R LENC CTRL0 RO	–	R	Bit[7:6]: Not used Bit[5]: Flip Bit[4]: Mirror Bit[3:2]: y_skip Bit[1:0]: x_skip
0x2B15	R LENC CTRL1 RO	–	R	Bit[7:2]: Not used Bit[1]: overflow_v Bit[0]: overflow_h
0x2B16	M NQ	–	R	Bit[7]: Not used Bit[6:0]: m_nq[6:0]

6.30 PD mapping control [0x5500 - 0x55FF]

table 6-30 PD mapping control registers (sheet 1 of 10)

address	register name	default value	R/W	description
0x5500	PDC MAP00	0x00	RW	Bit[7:0]: pdc_map00[31:24]
0x5501	PDC MAP00	0x80	RW	Bit[7:0]: pdc_map00[23:16]
0x5502	PDC MAP00	0x00	RW	Bit[7:0]: pdc_map00[15:8]
0x5503	PDC MAP00	0x00	RW	Bit[7:0]: pdc_map00[7:0]
0x5504	PDC MAP01	0x00	RW	Bit[7:0]: pdc_map01[31:24]
0x5505	PDC MAP01	0x40	RW	Bit[7:0]: pdc_map01[23:16]
0x5506	PDC MAP01	0x00	RW	Bit[7:0]: pdc_map01[15:8]

table 6-30 PD mapping control registers (sheet 2 of 10)

address	register name	default value	R/W	description
0x5507	PDC MAP01	0x00	RW	Bit[7:0]: pdc_map01[7:0]
0x5508	PDC MAP02	0x40	RW	Bit[7:0]: pdc_map02[31:24]
0x5509	PDC MAP02	0x40	RW	Bit[7:0]: pdc_map02[23:16]
0x550A	PDC MAP02	0x40	RW	Bit[7:0]: pdc_map02[15:8]
0x550B	PDC MAP02	0x40	RW	Bit[7:0]: pdc_map02[7:0]
0x550C	PDC MAP03	0x20	RW	Bit[7:0]: pdc_map03[31:24]
0x550D	PDC MAP03	0x20	RW	Bit[7:0]: pdc_map03[23:16]
0x550E	PDC MAP03	0x20	RW	Bit[7:0]: pdc_map03[15:8]
0x550F	PDC MAP03	0x20	RW	Bit[7:0]: pdc_map03[7:0]
0x5510	PDC MAP04	0x00	RW	Bit[7:0]: pdc_map04[31:24]
0x5511	PDC MAP04	0x00	RW	Bit[7:0]: pdc_map04[23:16]
0x5512	PDC MAP04	0x00	RW	Bit[7:0]: pdc_map04[15:8]
0x5513	PDC MAP04	0x00	RW	Bit[7:0]: pdc_map04[7:0]
0x5514	PDC MAP05	0x00	RW	Bit[7:0]: pdc_map05[31:24]
0x5515	PDC MAP05	0x00	RW	Bit[7:0]: pdc_map05[23:16]
0x5516	PDC MAP05	0x00	RW	Bit[7:0]: pdc_map05[15:8]
0x5517	PDC MAP05	0x00	RW	Bit[7:0]: pdc_map05[7:0]
0x5518	PDC MAP06	0x00	RW	Bit[7:0]: pdc_map06[31:24]
0x5519	PDC MAP06	0x00	RW	Bit[7:0]: pdc_map06[23:16]
0x551A	PDC MAP06	0x00	RW	Bit[7:0]: pdc_map06[15:8]
0x551B	PDC MAP06	0x00	RW	Bit[7:0]: pdc_map06[7:0]
0x551C	PDC MAP07	0x00	RW	Bit[7:0]: pdc_map07[31:24]
0x551D	PDC MAP07	0x00	RW	Bit[7:0]: pdc_map07[23:16]
0x551E	PDC MAP07	0x00	RW	Bit[7:0]: pdc_map07[15:8]
0x551F	PDC MAP07	0x00	RW	Bit[7:0]: pdc_map07[7:0]
0x5520	PDC MAP08	0x08	RW	Bit[7:0]: pdc_map08[31:24]
0x5521	PDC MAP08	0x00	RW	Bit[7:0]: pdc_map08[23:16]
0x5522	PDC MAP08	0x00	RW	Bit[7:0]: pdc_map08[15:8]
0x5523	PDC MAP08	0x00	RW	Bit[7:0]: pdc_map08[7:0]
0x5524	PDC MAP09	0x00	RW	Bit[7:0]: pdc_map09[31:24]

table 6-30 PD mapping control registers (sheet 3 of 10)

address	register name	default value	R/W	description
0x5525	PDC MAP09	0x00	RW	Bit[7:0]: pdc_map09[23:16]
0x5526	PDC MAP09	0x00	RW	Bit[7:0]: pdc_map09[15:8]
0x5527	PDC MAP09	0x00	RW	Bit[7:0]: pdc_map09[7:0]
0x5528	PDC MAP10	0x40	RW	Bit[7:0]: pdc_map10[31:24]
0x5529	PDC MAP10	0x40	RW	Bit[7:0]: pdc_map10[23:16]
0x552A	PDC MAP10	0x40	RW	Bit[7:0]: pdc_map10[15:8]
0x552B	PDC MAP10	0x40	RW	Bit[7:0]: pdc_map10[7:0]
0x552C	PDC MAP11	0x20	RW	Bit[7:0]: pdc_map11[31:24]
0x552D	PDC MAP11	0x20	RW	Bit[7:0]: pdc_map11[23:16]
0x552E	PDC MAP11	0x20	RW	Bit[7:0]: pdc_map11[15:8]
0x552F	PDC MAP11	0x20	RW	Bit[7:0]: pdc_map11[7:0]
0x5530	PDC MAP12	0x00	RW	Bit[7:0]: pdc_map12[31:24]
0x5531	PDC MAP12	0x00	RW	Bit[7:0]: pdc_map12[23:16]
0x5532	PDC MAP12	0x00	RW	Bit[7:0]: pdc_map12[15:8]
0x5533	PDC MAP12	0x00	RW	Bit[7:0]: pdc_map12[7:0]
0x5534	PDC MAP13	0x00	RW	Bit[7:0]: pdc_map13[31:24]
0x5535	PDC MAP13	0x00	RW	Bit[7:0]: pdc_map13[23:16]
0x5536	PDC MAP13	0x00	RW	Bit[7:0]: pdc_map13[15:8]
0x5537	PDC MAP13	0x00	RW	Bit[7:0]: pdc_map13[7:0]
0x5538	PDC MAP14	0x00	RW	Bit[7:0]: pdc_map14[31:24]
0x5539	PDC MAP14	0x00	RW	Bit[7:0]: pdc_map14[23:16]
0x553A	PDC MAP14	0x00	RW	Bit[7:0]: pdc_map14[15:8]
0x553B	PDC MAP14	0x00	RW	Bit[7:0]: pdc_map14[7:0]
0x553C	PDC MAP15	0x00	RW	Bit[7:0]: pdc_map15[31:24]
0x553D	PDC MAP15	0x00	RW	Bit[7:0]: pdc_map15[23:16]
0x553E	PDC MAP15	0x00	RW	Bit[7:0]: pdc_map15[15:8]
0x553F	PDC MAP15	0x00	RW	Bit[7:0]: pdc_map15[7:0]
0x5540	PDC MAP16	0x00	RW	Bit[7:0]: pdc_map16[31:24]
0x5541	PDC MAP16	0x00	RW	Bit[7:0]: pdc_map16[23:16]
0x5542	PDC MAP16	0x00	RW	Bit[7:0]: pdc_map16[15:8]

table 6-30 PD mapping control registers (sheet 4 of 10)

address	register name	default value	R/W	description
0x5543	PDC MAP16	0x00	RW	Bit[7:0]: pdc_map16[7:0]
0x5544	PDC MAP17	0x00	RW	Bit[7:0]: pdc_map17[31:24]
0x5545	PDC MAP17	0x00	RW	Bit[7:0]: pdc_map17[23:16]
0x5546	PDC MAP17	0x00	RW	Bit[7:0]: pdc_map17[15:8]
0x5547	PDC MAP17	0x00	RW	Bit[7:0]: pdc_map17[7:0]
0x5548	PDC MAP18	0x40	RW	Bit[7:0]: pdc_map18[31:24]
0x5549	PDC MAP18	0x40	RW	Bit[7:0]: pdc_map18[23:16]
0x554A	PDC MAP18	0x40	RW	Bit[7:0]: pdc_map18[15:8]
0x554B	PDC MAP18	0x40	RW	Bit[7:0]: pdc_map18[7:0]
0x554C	PDC MAP19	0x20	RW	Bit[7:0]: pdc_map19[31:24]
0x554D	PDC MAP19	0x20	RW	Bit[7:0]: pdc_map19[23:16]
0x554E	PDC MAP19	0x20	RW	Bit[7:0]: pdc_map19[15:8]
0x554F	PDC MAP19	0x20	RW	Bit[7:0]: pdc_map19[7:0]
0x5550	PDC MAP20	0x00	RW	Bit[7:0]: pdc_map20[31:24]
0x5551	PDC MAP20	0x00	RW	Bit[7:0]: pdc_map20[23:16]
0x5552	PDC MAP20	0x00	RW	Bit[7:0]: pdc_map20[15:8]
0x5553	PDC MAP20	0x00	RW	Bit[7:0]: pdc_map20[7:0]
0x5554	PDC MAP21	0x00	RW	Bit[7:0]: pdc_map21[31:24]
0x5555	PDC MAP21	0x00	RW	Bit[7:0]: pdc_map21[23:16]
0x5556	PDC MAP21	0x00	RW	Bit[7:0]: pdc_map21[15:8]
0x5557	PDC MAP21	0x00	RW	Bit[7:0]: pdc_map21[7:0]
0x5558	PDC MAP22	0x00	RW	Bit[7:0]: pdc_map22[31:24]
0x5559	PDC MAP22	0x00	RW	Bit[7:0]: pdc_map22[23:16]
0x555A	PDC MAP22	0x00	RW	Bit[7:0]: pdc_map22[15:8]
0x555B	PDC MAP22	0x00	RW	Bit[7:0]: pdc_map22[7:0]
0x555C	PDC MAP23	0x00	RW	Bit[7:0]: pdc_map23[31:24]
0x555D	PDC MAP23	0x00	RW	Bit[7:0]: pdc_map23[23:16]
0x555E	PDC MAP23	0x00	RW	Bit[7:0]: pdc_map23[15:8]
0x555F	PDC MAP23	0x00	RW	Bit[7:0]: pdc_map23[7:0]
0x5560	PDC MAP24	0x00	RW	Bit[7:0]: pdc_map24[31:24]

table 6-30 PD mapping control registers (sheet 5 of 10)

address	register name	default value	R/W	description
0x5561	PDC MAP24	0x00	RW	Bit[7:0]: pdc_map24[23:16]
0x5562	PDC MAP24	0x00	RW	Bit[7:0]: pdc_map24[15:8]
0x5563	PDC MAP24	0x08	RW	Bit[7:0]: pdc_map24[7:0]
0x5564	PDC MAP25	0x40	RW	Bit[7:0]: pdc_map25[31:24]
0x5565	PDC MAP25	0x00	RW	Bit[7:0]: pdc_map25[23:16]
0x5566	PDC MAP25	0x00	RW	Bit[7:0]: pdc_map25[15:8]
0x5567	PDC MAP25	0x00	RW	Bit[7:0]: pdc_map25[7:0]
0x5568	PDC MAP26	0x40	RW	Bit[7:0]: pdc_map26[31:24]
0x5569	PDC MAP26	0x40	RW	Bit[7:0]: pdc_map26[23:16]
0x556A	PDC MAP26	0x40	RW	Bit[7:0]: pdc_map26[15:8]
0x556B	PDC MAP26	0x40	RW	Bit[7:0]: pdc_map26[7:0]
0x556C	PDC MAP27	0x20	RW	Bit[7:0]: pdc_map27[31:24]
0x556D	PDC MAP27	0x20	RW	Bit[7:0]: pdc_map27[23:16]
0x556E	PDC MAP27	0x20	RW	Bit[7:0]: pdc_map27[15:8]
0x556F	PDC MAP27	0x20	RW	Bit[7:0]: pdc_map27[7:0]
0x5570	PDC MAP28	0x00	RW	Bit[7:0]: pdc_map28[31:24]
0x5571	PDC MAP28	0x00	RW	Bit[7:0]: pdc_map28[23:16]
0x5572	PDC MAP28	0x00	RW	Bit[7:0]: pdc_map28[15:8]
0x5573	PDC MAP28	0x00	RW	Bit[7:0]: pdc_map28[7:0]
0x5574	PDC MAP29	0x00	RW	Bit[7:0]: pdc_map29[31:24]
0x5575	PDC MAP29	0x00	RW	Bit[7:0]: pdc_map29[23:16]
0x5576	PDC MAP29	0x00	RW	Bit[7:0]: pdc_map29[15:8]
0x5577	PDC MAP29	0x00	RW	Bit[7:0]: pdc_map29[7:0]
0x5578	PDC MAP30	0x00	RW	Bit[7:0]: pdc_map30[31:24]
0x5579	PDC MAP30	0x00	RW	Bit[7:0]: pdc_map30[23:16]
0x557A	PDC MAP30	0x00	RW	Bit[7:0]: pdc_map30[15:8]
0x557B	PDC MAP30	0x00	RW	Bit[7:0]: pdc_map30[7:0]
0x557C	PDC MAP31	0x00	RW	Bit[7:0]: pdc_map31[31:24]
0x557D	PDC MAP31	0x00	RW	Bit[7:0]: pdc_map31[23:16]
0x557E	PDC MAP31	0x00	RW	Bit[7:0]: pdc_map31[15:8]

table 6-30 PD mapping control registers (sheet 6 of 10)

address	register name	default value	R/W	description
0x557F	PDC MAP31	0x00	RW	Bit[7:0]: pdc_map31[7:0]
0x5580	PDF MAP00	0x00	RW	Bit[7:0]: pdf_map00[31:24]
0x5581	PDF MAP00	0x00	RW	Bit[7:0]: pdf_map00[23:16]
0x5582	PDF MAP00	0x00	RW	Bit[7:0]: pdf_map00[15:8]
0x5583	PDF MAP00	0x00	RW	Bit[7:0]: pdf_map00[7:0]
0x5584	PDF MAP01	0x00	RW	Bit[7:0]: pdf_map01[31:24]
0x5585	PDF MAP01	0x00	RW	Bit[7:0]: pdf_map01[23:16]
0x5586	PDF MAP01	0x00	RW	Bit[7:0]: pdf_map01[15:8]
0x5587	PDF MAP01	0x00	RW	Bit[7:0]: pdf_map01[7:0]
0x5588	PDF MAP02	0x40	RW	Bit[7:0]: pdf_map02[31:24]
0x5589	PDF MAP02	0x40	RW	Bit[7:0]: pdf_map02[23:16]
0x558A	PDF MAP02	0x40	RW	Bit[7:0]: pdf_map02[15:8]
0x558B	PDF MAP02	0x40	RW	Bit[7:0]: pdf_map02[7:0]
0x558C	PDF MAP03	0x20	RW	Bit[7:0]: pdf_map03[31:24]
0x558D	PDF MAP03	0x20	RW	Bit[7:0]: pdf_map03[23:16]
0x558E	PDF MAP03	0x20	RW	Bit[7:0]: pdf_map03[15:8]
0x558F	PDF MAP03	0x20	RW	Bit[7:0]: pdf_map03[7:0]
0x5590	PDF MAP04	0x00	RW	Bit[7:0]: pdf_map04[31:24]
0x5591	PDF MAP04	0x00	RW	Bit[7:0]: pdf_map04[23:16]
0x5592	PDF MAP04	0x00	RW	Bit[7:0]: pdf_map04[15:8]
0x5593	PDF MAP04	0x00	RW	Bit[7:0]: pdf_map04[7:0]
0x5594	PDF MAP05	0x00	RW	Bit[7:0]: pdf_map05[31:24]
0x5595	PDF MAP05	0x00	RW	Bit[7:0]: pdf_map05[23:16]
0x5596	PDF MAP05	0x00	RW	Bit[7:0]: pdf_map05[15:8]
0x5597	PDF MAP05	0x00	RW	Bit[7:0]: pdf_map05[7:0]
0x5598	PDF MAP06	0x00	RW	Bit[7:0]: pdf_map06[31:24]
0x5599	PDF MAP06	0x00	RW	Bit[7:0]: pdf_map06[23:16]
0x559A	PDF MAP06	0x00	RW	Bit[7:0]: pdf_map06[15:8]
0x559B	PDF MAP06	0x00	RW	Bit[7:0]: pdf_map06[7:0]
0x559C	PDF MAP07	0x00	RW	Bit[7:0]: pdf_map07[31:24]

table 6-30 PD mapping control registers (sheet 7 of 10)

address	register name	default value	R/W	description
0x559D	PDF MAP07	0x00	RW	Bit[7:0]: pdf_map07[23:16]
0x559E	PDF MAP07	0x00	RW	Bit[7:0]: pdf_map07[15:8]
0x559F	PDF MAP07	0x00	RW	Bit[7:0]: pdf_map07[7:0]
0x55A0	PDF MAP08	0x00	RW	Bit[7:0]: pdf_map08[31:24]
0x55A1	PDF MAP08	0x00	RW	Bit[7:0]: pdf_map08[23:16]
0x55A2	PDF MAP08	0x00	RW	Bit[7:0]: pdf_map08[15:8]
0x55A3	PDF MAP08	0x00	RW	Bit[7:0]: pdf_map08[7:0]
0x55A4	PDF MAP09	0x00	RW	Bit[7:0]: pdf_map09[31:24]
0x55A5	PDF MAP09	0x00	RW	Bit[7:0]: pdf_map09[23:16]
0x55A6	PDF MAP09	0x00	RW	Bit[7:0]: pdf_map09[15:8]
0x55A7	PDF MAP09	0x00	RW	Bit[7:0]: pdf_map09[7:0]
0x55A8	PDF MAP10	0x40	RW	Bit[7:0]: pdf_map10[31:24]
0x55A9	PDF MAP10	0x40	RW	Bit[7:0]: pdf_map10[23:16]
0x55AA	PDF MAP10	0x40	RW	Bit[7:0]: pdf_map10[15:8]
0x55AB	PDF MAP10	0x40	RW	Bit[7:0]: pdf_map10[7:0]
0x55AC	PDF MAP11	0x20	RW	Bit[7:0]: pdf_map11[31:24]
0x55AD	PDF MAP11	0x20	RW	Bit[7:0]: pdf_map11[23:16]
0x55AE	PDF MAP11	0x20	RW	Bit[7:0]: pdf_map11[15:8]
0x55AF	PDF MAP11	0x20	RW	Bit[7:0]: pdf_map11[7:0]
0x55B0	PDF MAP12	0x00	RW	Bit[7:0]: pdf_map12[31:24]
0x55B1	PDF MAP12	0x00	RW	Bit[7:0]: pdf_map12[23:16]
0x55B2	PDF MAP12	0x00	RW	Bit[7:0]: pdf_map12[15:8]
0x55B3	PDF MAP12	0x00	RW	Bit[7:0]: pdf_map12[7:0]
0x55B4	PDF MAP13	0x00	RW	Bit[7:0]: pdf_map13[31:24]
0x55B5	PDF MAP13	0x00	RW	Bit[7:0]: pdf_map13[23:16]
0x55B6	PDF MAP13	0x00	RW	Bit[7:0]: pdf_map13[15:8]
0x55B7	PDF MAP13	0x00	RW	Bit[7:0]: pdf_map13[7:0]
0x55B8	PDF MAP14	0x00	RW	Bit[7:0]: pdf_map14[31:24]
0x55B9	PDF MAP14	0x00	RW	Bit[7:0]: pdf_map14[23:16]
0x55BA	PDF MAP14	0x00	RW	Bit[7:0]: pdf_map14[15:8]

table 6-30 PD mapping control registers (sheet 8 of 10)

address	register name	default value	R/W	description
0x55BB	PDF MAP14	0x00	RW	Bit[7:0]: pdf_map14[7:0]
0x55BC	PDF MAP15	0x00	RW	Bit[7:0]: pdf_map15[31:24]
0x55BD	PDF MAP15	0x00	RW	Bit[7:0]: pdf_map15[23:16]
0x55BE	PDF MAP15	0x00	RW	Bit[7:0]: pdf_map15[15:8]
0x55BF	PDF MAP15	0x00	RW	Bit[7:0]: pdf_map15[7:0]
0x55C0	PDF MAP16	0x00	RW	Bit[7:0]: pdf_map16[31:24]
0x55C1	PDF MAP16	0x00	RW	Bit[7:0]: pdf_map16[23:16]
0x55C2	PDF MAP16	0x00	RW	Bit[7:0]: pdf_map16[15:8]
0x55C3	PDF MAP16	0x00	RW	Bit[7:0]: pdf_map16[7:0]
0x55C4	PDF MAP17	0x00	RW	Bit[7:0]: pdf_map17[31:24]
0x55C5	PDF MAP17	0x00	RW	Bit[7:0]: pdf_map17[23:16]
0x55C6	PDF MAP17	0x00	RW	Bit[7:0]: pdf_map17[15:8]
0x55C7	PDF MAP17	0x00	RW	Bit[7:0]: pdf_map17[7:0]
0x55C8	PDF MAP18	0x40	RW	Bit[7:0]: pdf_map18[31:24]
0x55C9	PDF MAP18	0x40	RW	Bit[7:0]: pdf_map18[23:16]
0x55CA	PDF MAP18	0x40	RW	Bit[7:0]: pdf_map18[15:8]
0x55CB	PDF MAP18	0x40	RW	Bit[7:0]: pdf_map18[7:0]
0x55CC	PDF MAP19	0x20	RW	Bit[7:0]: pdf_map19[31:24]
0x55CD	PDF MAP19	0x20	RW	Bit[7:0]: pdf_map19[23:16]
0x55CE	PDF MAP19	0x20	RW	Bit[7:0]: pdf_map19[15:8]
0x55CF	PDF MAP19	0x20	RW	Bit[7:0]: pdf_map19[7:0]
0x55D0	PDF MAP20	0x00	RW	Bit[7:0]: pdf_map20[31:24]
0x55D1	PDF MAP20	0x00	RW	Bit[7:0]: pdf_map20[23:16]
0x55D2	PDF MAP20	0x00	RW	Bit[7:0]: pdf_map20[15:8]
0x55D3	PDF MAP20	0x00	RW	Bit[7:0]: pdf_map20[7:0]
0x55D4	PDF MAP21	0x00	RW	Bit[7:0]: pdf_map21[31:24]
0x55D5	PDF MAP21	0x00	RW	Bit[7:0]: pdf_map21[23:16]
0x55D6	PDF MAP21	0x00	RW	Bit[7:0]: pdf_map21[15:8]
0x55D7	PDF MAP21	0x00	RW	Bit[7:0]: pdf_map21[7:0]
0x55D8	PDF MAP22	0x00	RW	Bit[7:0]: pdf_map22[31:24]

table 6-30 PD mapping control registers (sheet 9 of 10)

address	register name	default value	R/W	description
0x55D9	PDF MAP22	0x00	RW	Bit[7:0]: pdf_map22[23:16]
0x55DA	PDF MAP22	0x00	RW	Bit[7:0]: pdf_map22[15:8]
0x55DB	PDF MAP22	0x00	RW	Bit[7:0]: pdf_map22[7:0]
0x55DC	PDF MAP23	0x00	RW	Bit[7:0]: pdf_map23[31:24]
0x55DD	PDF MAP23	0x00	RW	Bit[7:0]: pdf_map23[23:16]
0x55DE	PDF MAP23	0x00	RW	Bit[7:0]: pdf_map23[15:8]
0x55DF	PDF MAP23	0x00	RW	Bit[7:0]: pdf_map23[7:0]
0x55E0	PDF MAP24	0x00	RW	Bit[7:0]: pdf_map24[31:24]
0x55E1	PDF MAP24	0x00	RW	Bit[7:0]: pdf_map24[23:16]
0x55E2	PDF MAP24	0x00	RW	Bit[7:0]: pdf_map24[15:8]
0x55E3	PDF MAP24	0x00	RW	Bit[7:0]: pdf_map24[7:0]
0x55E4	PDF MAP25	0x00	RW	Bit[7:0]: pdf_map25[31:24]
0x55E5	PDF MAP25	0x00	RW	Bit[7:0]: pdf_map25[23:16]
0x55E6	PDF MAP25	0x00	RW	Bit[7:0]: pdf_map25[15:8]
0x55E7	PDF MAP25	0x00	RW	Bit[7:0]: pdf_map25[7:0]
0x55E8	PDF MAP26	0x40	RW	Bit[7:0]: pdf_map26[31:24]
0x55E9	PDF MAP26	0x40	RW	Bit[7:0]: pdf_map26[23:16]
0x55EA	PDF MAP26	0x40	RW	Bit[7:0]: pdf_map26[15:8]
0x55EB	PDF MAP26	0x40	RW	Bit[7:0]: pdf_map26[7:0]
0x55EC	PDF MAP27	0x20	RW	Bit[7:0]: pdf_map27[31:24]
0x55ED	PDF MAP27	0x20	RW	Bit[7:0]: pdf_map27[23:16]
0x55EE	PDF MAP27	0x20	RW	Bit[7:0]: pdf_map27[15:8]
0x55EF	PDF MAP27	0x20	RW	Bit[7:0]: pdf_map27[7:0]
0x55F0	PDF MAP28	0x00	RW	Bit[7:0]: pdf_map28[31:24]
0x55F1	PDF MAP28	0x00	RW	Bit[7:0]: pdf_map28[23:16]
0x55F2	PDF MAP28	0x00	RW	Bit[7:0]: pdf_map28[15:8]
0x55F3	PDF MAP28	0x00	RW	Bit[7:0]: pdf_map28[7:0]
0x55F4	PDF MAP29	0x00	RW	Bit[7:0]: pdf_map29[31:24]
0x55F5	PDF MAP29	0x00	RW	Bit[7:0]: pdf_map29[23:16]
0x55F6	PDF MAP29	0x00	RW	Bit[7:0]: pdf_map29[15:8]

table 6-30 PD mapping control registers (sheet 10 of 10)

address	register name	default value	R/W	description
0x55F7	PDF MAP29	0x00	RW	Bit[7:0]: pdf_map29[7:0]
0x55F8	PDF MAP30	0x00	RW	Bit[7:0]: pdf_map30[31:24]
0x55F9	PDF MAP30	0x00	RW	Bit[7:0]: pdf_map30[23:16]
0x55FA	PDF MAP30	0x00	RW	Bit[7:0]: pdf_map30[15:8]
0x55FB	PDF MAP30	0x00	RW	Bit[7:0]: pdf_map30[7:0]
0x55FC	PDF MAP31	0x00	RW	Bit[7:0]: pdf_map31[31:24]
0x55FD	PDF MAP31	0x00	RW	Bit[7:0]: pdf_map31[23:16]
0x55FE	PDF MAP31	0x00	RW	Bit[7:0]: pdf_map31[15:8]
0x55FF	PDF MAP31	0x00	RW	Bit[7:0]: pdf_map31[7:0]

6.31 PDC control [0x5D00 - 0x5D32, 0x5D34 - 0x5D3A, 0x5D40 - 0x5D44]

table 6-31 PDC control registers (sheet 1 of 4)

address	register name	default value	R/W	description
0x5D00	REVERSE RATIO 0	0x01	RW	Bit[7:0]: reverse_ratio_0[15:8]
0x5D01	REVERSE RATIO 0	0x00	RW	Bit[7:0]: reverse_ratio_0[7:0]
0x5D02	REVERSE RATIO 1	0x01	RW	Bit[7:0]: reverse_ratio_1[15:8]
0x5D03	REVERSE RATIO 1	0x00	RW	Bit[7:0]: reverse_ratio_1[7:0]
0x5D04	REVERSE RATIO 2	0x01	RW	Bit[7:0]: reverse_ratio_2[15:8]
0x5D05	REVERSE RATIO 2	0x47	RW	Bit[7:0]: reverse_ratio_2[7:0]
0x5D06	REVERSE RATIO 3	0x01	RW	Bit[7:0]: reverse_ratio_3[15:8]
0x5D07	REVERSE RATIO 3	0x47	RW	Bit[7:0]: reverse_ratio_3[7:0]
0x5D08	FADING LIST0 0	0x70	RW	Bit[7:0]: fading_list0_0
0x5D09	FADING LIST0 1	0x74	RW	Bit[7:0]: fading_list0_1
0x5D0A	FADING LIST0 2	0x78	RW	Bit[7:0]: fading_list0_2
0x5D0B	FADING LIST0 3	0x7C	RW	Bit[7:0]: fading_list0_3
0x5D0C	FADING LIST0 4	0x80	RW	Bit[7:0]: fading_list0_4
0x5D0D	FADING LIST1 0	0x80	RW	Bit[7:0]: fading_list1_0

table 6-31 PDC control registers (sheet 2 of 4)

address	register name	default value	R/W	description
0x5D0E	FADING LIST1 1	0x7C	RW	Bit[7:0]: fading_list1_1
0x5D0F	FADING LIST1 2	0x78	RW	Bit[7:0]: fading_list1_2
0x5D10	FADING LIST1 3	0x74	RW	Bit[7:0]: fading_list1_3
0x5D11	FADING LIST1 4	0x70	RW	Bit[7:0]: fading_list1_4
0x5D12	FADING LIST2 0	0x70	RW	Bit[7:0]: fading_list2_0
0x5D13	FADING LIST2 1	0x74	RW	Bit[7:0]: fading_list2_1
0x5D14	FADING LIST2 2	0x78	RW	Bit[7:0]: fading_list2_2
0x5D15	FADING LIST2 3	0x7C	RW	Bit[7:0]: fading_list2_3
0x5D16	FADING LIST2 4	0x80	RW	Bit[7:0]: fading_list2_4
0x5D17	FADING LIST3 0	0x80	RW	Bit[7:0]: fading_list3_0
0x5D18	FADING LIST3 1	0x7C	RW	Bit[7:0]: fading_list3_1
0x5D19	FADING LIST3 2	0x78	RW	Bit[7:0]: fading_list3_2
0x5D1A	FADING LIST3 3	0x74	RW	Bit[7:0]: fading_list3_3
0x5D1B	FADING LIST3 4	0x70	RW	Bit[7:0]: fading_list3_4
0x5D1C	FOCUS WIN LEFT	0x00	RW	Bit[7:5]: Not used Bit[4:0]: focus_win_left[12:8]
0x5D1D	FOCUS WIN LEFT	0x00	RW	Bit[7:0]: focus_win_left[7:0]
0x5D1E	FOCUS WIN TOP	0x00	RW	Bit[7:5]: Not used Bit[4:0]: focus_win_top[12:8]
0x5D1F	FOCUS WIN TOP	0x00	RW	Bit[7:0]: focus_win_top[7:0]
0x5D20	FOCUS WIN WIDTH	0x16	RW	Bit[7:5]: Not used Bit[4:0]: focus_win_width[12:8]
0x5D21	FOCUS WIN WIDTH	0x20	RW	Bit[7:0]: focus_win_width[7:0]
0x5D22	FOCUS WIN HEIGHT	0x10	RW	Bit[7:5]: Not used Bit[4:0]: focus_win_height[12:8]
0x5D23	FOCUS WIN HEIGHT	0xA0	RW	Bit[7:0]: focus_win_height[7:0]
0x5D24	X OFFSET MAN	0x00	RW	Bit[7:5]: Not used Bit[4:0]: x_offset_man[12:8]
0x5D25	X OFFSET MAN	0x00	RW	Bit[7:0]: x_offset_man[7:0]
0x5D26	Y OFFSET MAN	0x00	RW	Bit[7:5]: Not used Bit[4:0]: y_offset_man[12:8]
0x5D27	Y OFFSET MAN	0x00	RW	Bit[7:0]: y_offset_man[7:0]

table 6-31 PDC control registers (sheet 3 of 4)

address	register name	default value	R/W	description
0x5D28	R PDC CTRL1 RW	0x80	RW	Bit[7]: blc_en Bit[6]: offset_man_en Bit[5]: v_bin_man_en Bit[4]: v_bin_man Bit[3]: mirror_man_en Bit[2]: mirror_man Bit[1]: flip_man_en Bit[0]: flip_man
0x5D29	R PDC CTRL2 RW	0x00	RW	Bit[7]: before_comp_en Bit[6]: focus_win_en Bit[5]: h_bin_man_en Bit[4]: h_bin_man Bit[3]: fix_ptn_en Bit[2]: fix_ptn_mode Bit[1]: h_bin4_en Bit[0]: v_bin4_en
0x5D2A	STARTH	0x02	RW	Bit[7:5]: Not used Bit[4:0]: Starth[12:8]
0x5D2B	STARTH	0x30	RW	Bit[7:0]: Starth[7:0]
0x5D2C	STOPH	0x12	RW	Bit[7:5]: Not used Bit[4:0]: Stoph[12:8]
0x5D2D	STOPH	0x30	RW	Bit[7:0]: Stoph[7:0]
0x5D2E	STARTV	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Startv[12:8]
0x5D2F	STARTV	0x28	RW	Bit[7:0]: Startv[7:0]
0x5D30	STOPV	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: Stopv[12:8]
0x5D31	STOPV	0xA8	RW	Bit[7:0]: Stopv[7:0]
0x5D32	R PDC CTRL3 RW	0x00	RW	Bit[7]: Not used Bit[6]: zone_man_en Bit[5]: bypass_ratio Bit[4]: rl_channel3 Bit[3]: Ratio mirror manual enable Bit[2]: Ratio mirror manual Bit[1]: Ratio flip manual enable Bit[0]: Ratio flip manual
0x5D34	ARRAY W	0x12	RW	Bit[7:5]: Not used Bit[4:0]: array_w[12:8]
0x5D35	ARRAY W	0x60	RW	Bit[7:0]: array_w[7:0]
0x5D36	ARRAY H	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: array_h[12:8]

table 6-31 PDC control registers (sheet 4 of 4)

address	register name	default value	R/W	description
0x5D37	ARRAY H	0xD0	RW	Bit[7:0]: array_h[7:0]
0x5D38	FADING SCALERH	0x5D	RW	Bit[7:0]: fading_scalerh
0x5D39	FADING SCALERV	0x7C	RW	Bit[7:0]: fading_scalerv
0x5D3A	PATTERN 6	0x08	RW	Bit[7:0]: For pattern #6
0x5D40	X OFFSET	–	R	Bit[7:5]: Not used Bit[4:0]: x_offset[12:8]
0x5D41	X OFFSET	–	R	Bit[7:0]: x_offset[7:0]
0x5D42	Y OFFSET	–	R	Bit[7:5]: Not used Bit[4:0]: y_offset[12:8]
0x5D43	Y OFFSET	–	R	Bit[7:0]: y_offset[7:0]
0x5D44	R PDC CTRL RO	–	R	Bit[7:4]: Not used Bit[3]: h_bin_en Bit[2]: v_bin_en Bit[1]: Mirror Bit[0]: Flip

6.32 DPC control [0x5600 - 0x561A, 0x5620 - 0x56A5]

table 6-32 DPC control registers (sheet 1 of 8)

address	register name	default value	R/W	description
0x5600	R CTRL00	0x30	RW	Bit[7:6]: Not used Bit[5]: dpc1_white_en Bit[4]: dpc1_black_en Bit[3]: Not used Bit[2]: dpc1_man_en Bit[1:0]: dpc1_level_man
0x5601	DPC1 WTHRELIST0	0x08	RW	Bit[7:0]: dpc1_wthrelist0[7:0]
0x5602	DPC1 WTHRELIST1	0x04	RW	Bit[7:0]: dpc1_wthrelist1[7:0]
0x5603	DPC1 WTHRELIST2	0x02	RW	Bit[7:0]: dpc1_wthrelist2[7:0]
0x5604	DPC1 BTHRELIST0	0x08	RW	Bit[7:0]: dpc1_bthrelist0[7:0]
0x5605	DPC1 BTHRELIST1	0x04	RW	Bit[7:0]: dpc1_bthrelist1[7:0]
0x5606	DPC1 BTHRELIST2	0x02	RW	Bit[7:0]: dpc1_bthrelist2[7:0]

table 6-32 DPC control registers (sheet 2 of 8)

address	register name	default value	R/W	description
0x5607	DPC1 RATIOLIST0	0x03	RW	Bit[7:4]: Not used Bit[3:0]: dpc1_ratiolist0[3:0]
0x5608	DPC1 RATIOLIST1	0x03	RW	Bit[7:4]: Not used Bit[3:0]: dpc1_ratiolist1[3:0]
0x5609	DPC1 RATIOLIST2	0x03	RW	Bit[7:4]: Not used Bit[3:0]: dpc1_ratiolist2[3:0]
0x560A	DPC1 GAINPIVOT0	0x06	RW	Bit[7:0]: dpc1_gainpivot0[7:0]
0x560B	DPC1 GAINPIVOT1	0x03	RW	Bit[7:0]: dpc1_gainpivot1[7:0]
0x560C	DPC1 GAINMARGIN	0x08	RW	Bit[7:5]: Not used Bit[4:0]: dpc1_gainmargin[4:0]
0x560D	R CTRL0D	0xFE	RW	Bit[7]: dpc1_en_swp3 Bit[6]: dpc1_en_swp2 Bit[5]: dpc1_en_swp1 Bit[4]: dpc1_en_swp0 Bit[3]: dpc1_en_cwp3 Bit[2]: dpc1_en_cwp2 Bit[1]: dpc1_en_cwp1 Bit[0]: dpc1_en_cwp0
0x560E	R CTRL0E	0x0C	RW	Bit[7:4]: Not used Bit[3]: dpc1_en_twp3 Bit[2]: dpc1_en_twp2 Bit[1]: dpc1_en_twp1 Bit[0]: dpc1_en_twp0
0x560F	R CTRL0F	0xE4	RW	Bit[7:6]: dpc1_dc_swp3 Bit[5:4]: dpc1_dc_swp2 Bit[3:2]: dpc1_dc_swp1 Bit[1:0]: dpc1_dc_swp0
0x5610	R CTRL10	0xD0	RW	Bit[7:6]: dpc1_dc_cwp3 Bit[5:4]: dpc1_dc_cwp2 Bit[3:2]: dpc1_dc_cwp1 Bit[1:0]: dpc1_dc_cwp0
0x5611	R CTRL11	0x00	RW	Bit[7:6]: dpc1_dc_twp3 Bit[5:4]: dpc1_dc_twp2 Bit[3:2]: dpc1_dc_twp1 Bit[1:0]: dpc1_dc_twp0

table 6-32 DPC control registers (sheet 3 of 8)

address	register name	default value	R/W	description
0x5612	R CTRL12	0x74	RW	Bit[7]: Not used Bit[6]: dpc1_en_sbp2 Bit[5]: dpc1_en_sbp1 Bit[4]: dpc1_en_sbp0 Bit[3]: Not used Bit[2]: dpc1_en_cbp2 Bit[1]: dpc1_en_cbp1 Bit[0]: dpc1_en_cbp0
0x5613	R CTRL13	0x06	RW	Bit[7]: Not used Bit[6]: dpc1_en_tbp2 Bit[5]: dpc1_en_tbp1 Bit[4]: dpc1_en_tbp0 Bit[3]: Not used Bit[2]: dpc1_en_vdc2 Bit[1]: dpc1_en_vdc1 Bit[0]: dpc1_en_vdc0
0x5614	R CTRL14	0x40	RW	Bit[7]: Not used Bit[6]: dpc1_en_cross2 Bit[5]: dpc1_en_cross1 Bit[4]: dpc1_en_cross0 Bit[3]: Not used Bit[2]: dpc1_dis_tri2 Bit[1]: dpc1_dis_tri1 Bit[0]: dpc1_dis_tri0
0x5615	R CTRL15	0x10	RW	Bit[7:6]: Not used Bit[5:4]: dpc1_dc_sbp2 Bit[3:2]: dpc1_dc_sbp1 Bit[1:0]: dpc1_dc_sbp0
0x5616	R CTRL16	0x00	RW	Bit[7:6]: Not used Bit[5:4]: dpc1_dc_cbp2 Bit[3:2]: dpc1_dc_cbp1 Bit[1:0]: dpc1_dc_cbp0
0x5617~ 0x5618	RSVD	–	–	Reserved
0x5619	DPC1 PTN THRE	0x06	RW	Bit[7:4]: Not used Bit[3:0]: dpc1_ptn_thre[3:0]
0x561A	R CTRL1A	0x33	RW	Bit[7:6]: Not used Bit[5]: dpc1_adv_rev Bit[4]: dpc1_en_ptn Bit[3:2]: Not used Bit[1:0]: dpc1_edge_opt
0x5620~ 0x565A	NOT USED	–	–	Not Used

table 6-32 DPC control registers (sheet 4 of 8)

address	register name	default value	R/W	description
0x565B~ 0x565F	RSVD	–	–	Reserved
0x5660	R CTRL00	0x30	RW	Bit[7:6]: Not used Bit[5]: dpc4_white_en Bit[4]: dpc4_black_en Bit[3]: Not used Bit[2]: dpc4_man_en Bit[1:0]: dpc4_level_man
0x5661	DPC4 WTHRELIST0	0x08	RW	Bit[7:0]: dpc4_wthrelist0[7:0]
0x5662	DPC4 WTHRELIST1	0x04	RW	Bit[7:0]: dpc4_wthrelist1[7:0]
0x5663	DPC4 WTHRELIST2	0x02	RW	Bit[7:0]: dpc4_wthrelist2[7:0]
0x5664	DPC4 BTHRELIST0	0x08	RW	Bit[7:0]: dpc4_bthrelist0[7:0]
0x5665	DPC4 BTHRELIST1	0x04	RW	Bit[7:0]: dpc4_bthrelist1[7:0]
0x5666	DPC4 BTHRELIST2	0x02	RW	Bit[7:0]: dpc4_bthrelist2[7:0]
0x5667	DPC4 RATIOLIST0	0x03	RW	Bit[7:4]: Not used Bit[3:0]: dpc4_ratiolist0[3:0]
0x5668	DPC4 RATIOLIST1	0x03	RW	Bit[7:4]: Not used Bit[3:0]: dpc4_ratiolist1[3:0]
0x5669	DPC4 RATIOLIST2	0x03	RW	Bit[7:4]: Not used Bit[3:0]: dpc4_ratiolist2[3:0]
0x566A	DPC4 GAINPIVOT0	0x06	RW	Bit[7:0]: dpc4_gainpivot0[7:0]
0x566B	DPC4 GAINPIVOT1	0x03	RW	Bit[7:0]: dpc4_gainpivot1[7:0]
0x566C	DPC4 GAINMARGIN	0x08	RW	Bit[7:5]: Not used Bit[4:0]: dpc4_gainmargin[4:0]
0x566D	R CTRL0D	0xFE	RW	Bit[7]: dpc4_en_swp3 Bit[6]: dpc4_en_swp2 Bit[5]: dpc4_en_swp1 Bit[4]: dpc4_en_swp0 Bit[3]: dpc4_en_cwp3 Bit[2]: dpc4_en_cwp2 Bit[1]: dpc4_en_cwp1 Bit[0]: dpc4_en_cwp0
0x566E	R CTRL0E	0x0C	RW	Bit[7:4]: Not used Bit[3]: dpc4_en_twp3 Bit[2]: dpc4_en_twp2 Bit[1]: dpc4_en_twp1 Bit[0]: dpc4_en_twp0

table 6-32 DPC control registers (sheet 5 of 8)

address	register name	default value	R/W	description
0x566F	R CTRL0F	0xE4	RW	Bit[7:6]: dpc4_dc_swp3 Bit[5:4]: dpc4_dc_swp2 Bit[3:2]: dpc4_dc_swp1 Bit[1:0]: dpc4_dc_swp0
0x5670	R CTRL10	0xD0	RW	Bit[7:6]: dpc4_dc_cwp3 Bit[5:4]: dpc4_dc_cwp2 Bit[3:2]: dpc4_dc_cwp1 Bit[1:0]: dpc4_dc_cwp0
0x5671	R CTRL11	0x00	RW	Bit[7:6]: dpc4_dc_twp3 Bit[5:4]: dpc4_dc_twp2 Bit[3:2]: dpc4_dc_twp1 Bit[1:0]: dpc4_dc_twp0
0x5672	R CTRL12	0x74	RW	Bit[7]: Not used Bit[6]: dpc4_en_sbp2 Bit[5]: dpc4_en_sbp1 Bit[4]: dpc4_en_sbp0 Bit[3]: Not used Bit[2]: dpc4_en_cbp2 Bit[1]: dpc4_en_cbp1 Bit[0]: dpc4_en_cbp0
0x5673	R CTRL13	0x06	RW	Bit[7]: Not used Bit[6]: dpc4_en_tbp2 Bit[5]: dpc4_en_tbp1 Bit[4]: dpc4_en_tbp0 Bit[3]: Not used Bit[2]: dpc4_en_vdc2 Bit[1]: dpc4_en_vdc1 Bit[0]: dpc4_en_vdc0
0x5674	R CTRL14	0x40	RW	Bit[7]: Not used Bit[6]: dpc4_en_cross2 Bit[5]: dpc4_en_cross1 Bit[4]: dpc4_en_cross0 Bit[3]: Not used Bit[2]: dpc4_dis_tri2 Bit[1]: dpc4_dis_tri1 Bit[0]: dpc4_dis_tri0
0x5675	R CTRL15	0x10	RW	Bit[7:6]: Not used Bit[5:4]: dpc4_dc_sbp2 Bit[3:2]: dpc4_dc_sbp1 Bit[1:0]: dpc4_dc_sbp0
0x5676	R CTRL16	0x00	RW	Bit[7:6]: Not used Bit[5:4]: dpc4_dc_cbp2 Bit[3:2]: dpc4_dc_cbp1 Bit[1:0]: dpc4_dc_cbp0

table 6-32 DPC control registers (sheet 6 of 8)

address	register name	default value	R/W	description
0x5677	R CTRL17	0x00	RW	Bit[7:6]: Not used Bit[5:4]: dpc4_dc_tbp2 Bit[3:2]: dpc4_dc_tbp1 Bit[1:0]: dpc4_dc_tbp0
0x5678	DPC4 SAT	0xFF	RW	Bit[7:0]: dpc4_sat[7:0]
0x5679	DPC4 PTN THRE	0x06	RW	Bit[7:4]: Not used Bit[3:0]: dpc4_ptn_thre[3:0]
0x567A	R CTRL7A	0x33	RW	Bit[7:6]: Not used Bit[5]: dpc4_adv_rev Bit[4]: dpc4_en_ptn Bit[3:2]: Not used Bit[1:0]: dpc4_edge_opt
0x567B	R CTRL7B	0x00	RW	Bit[7]: ptn_man_en Bit[6]: Not used Bit[5:4]: man_expo_mode Bit[3:2]: man_cfa_ptn Bit[1:0]: man_hdr_ptn
0x567C	R CTRL7C	0x00	RW	Bit[7]: pd_ptn_man_en Bit[6]: zone_man_en Bit[5:4]: pd_man_expo_mode Bit[3:2]: pd_man_cfa_ptn Bit[1:0]: pd_man_hdr_ptn
0x567D~ 0x567F	RSVD	–	–	Reserved
0x5680	RO WTHRE	–	R	Bit[7:0]: ro_wthre[7:0]
0x5681	RO BTHRE	–	R	Bit[7:0]: ro_bthre[7:0]
0x5682	RO RATIO	–	R	Bit[7:4]: Not used Bit[3:0]: ro_ratio[3:0]
0x5683	RO LEVEL	–	R	Bit[7:2]: Not used Bit[1:0]: ro_level[1:0]
0x5684	X OFFSET	–	R	Bit[7:5]: Not used Bit[4:0]: x_offset[12:8]
0x5685	X OFFSET	–	R	Bit[7:0]: x_offset[7:0]
0x5686	Y OFFSET	–	R	Bit[7:5]: Not used Bit[4:0]: y_offset[12:8]
0x5687	Y OFFSET	–	R	Bit[7:0]: y_offset[7:0]

table 6-32 DPC control registers (sheet 7 of 8)

address	register name	default value	R/W	description
0x5688	R PDF CTRL RO	–	R	Bit[7:4]: Not used Bit[3]: h_bin_en Bit[2]: v_bin_en Bit[1]: Mirror Bit[0]: Flip
0x5689~ 0x568F	RSVD	–	–	Reserved
0x5690	X OFFSET MAN	0x00	RW	Bit[7:5]: Not used Bit[4:0]: x_offset_man[12:8]
0x5691	X OFFSET MAN	0x00	RW	Bit[7:0]: x_offset_man[7:0]
0x5692	Y OFFSET MAN	0x00	RW	Bit[7:4]: Not used Bit[3:0]: y_offset_man[11:8]
0x5693	Y OFFSET MAN	0x00	RW	Bit[7:0]: y_offset_man[7:0]
0x5694	R PDF CTRL1	0x00	RW	Bit[7]: pd_remove_en Bit[6]: offset_man_en Bit[5]: v_bin_man_en Bit[4]: v_bin_man Bit[3]: mirror_man_en Bit[2]: mirror_man Bit[1]: flip_man_en Bit[0]: flip_man
0x5695	R PDF CTRL2	0x00	RW	Bit[7:6]: Not used Bit[5]: h_bin_man_en Bit[4]: h_bin_man Bit[3]: fix_ptn_en Bit[2]: fix_ptn_mode Bit[1:0]: mask_row_dis
0x5696	WEIGHT C	0x08	RW	Bit[7:5]: Not used Bit[4:0]: weight_c[4:0]
0x5697	WEIGHT D	0x08	RW	Bit[7:5]: Not used Bit[4:0]: weight_d[4:0]
0x5698	STARTH	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Starth[12:8]
0x5699	STARTH	0x30	RW	Bit[7:0]: Starth[7:0]
0x569A	STOPH	0x12	RW	Bit[7:5]: Not used Bit[4:0]: Stoph[12:8]
0x569B	STOPH	0x30	RW	Bit[7:0]: Stoph[7:0]
0x569C	STARTV	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Startv[12:8]
0x569D	STARTV	0x28	RW	Bit[7:0]: Startv[7:0]

table 6-32 DPC control registers (sheet 8 of 8)

address	register name	default value	R/W	description
0x569E	STOPV	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: Stopv[12:8]
0x569F	STOPV	0xA8	RW	Bit[7:0]: Stopv[7:0]
0x56A0	R PDF CTRL5	0x16	RW	Bit[7]: dis_d2_to_d4 Bit[6]: odd_green_rvs Bit[5]: rl_channel3 Bit[4]: ext_en Bit[3:2]: ext_ptn3 Bit[1:0]: ext_ptn4
0x56A1	SHADOW TH	0xC0	RW	Bit[7]: Not used Bit[6:0]: shadow_th[6:0]
0x56A2	ARRAY W	0x12	RW	Bit[7:5]: Not used Bit[4:0]: array_w[12:8]
0x56A3	ARRAY W	0x60	RW	Bit[7:0]: array_w[7:0]
0x56A4	ARRAY H	0x0D	RW	Bit[7:5]: Not used Bit[4:0]: array_h[12:8]
0x56A5	ARRAY H	0xD0	RW	Bit[7:0]: array_h[7:0]

6.33 window [0x5C00 - 0x5C0C, 0x5C80 - 0x5C8D, 0x5CA0 - 0x5CA6, 0x5C90 - 0x5C97]

table 6-33 window control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5C00	XSTART	0x00	RW	Bit[7:5]: Not used Bit[4:0]: Xstart[12:8] Start address in horizontal
0x5C01	XSTART	0x00	RW	Bit[7:0]: Xstart[7:0] Start address in horizontal
0x5C02	YSTART	0x00	RW	Bit[7:4]: Not used Bit[3:0]: Ystart[11:8] Start address in vertical
0x5C03	YSTART	0x00	RW	Bit[7:0]: Ystart[7:0] Start address in vertical

table 6-33 window control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5C04	X WIN	0x12	RW	Bit[7:5]: Not used Bit[4:0]: x_win[12:8] Select window width
0x5C05	X WIN	0x00	RW	Bit[7:0]: x_win[7:0] Select window width
0x5C06	Y WIN	0x0D	RW	Bit[7:4]: Not used Bit[3:0]: y_win[11:8] Select window height
0x5C07	Y WIN	0x80	RW	Bit[7:0]: y_win[7:0] Select window height
0x5C08	WIN MAN EN	0x00	RW	Bit[7:4]: Embedded line number Bit[2]: Embedded line position 0: At beginning of image frame 1: At end of image frame Bit[1]: Not used Bit[0]: win_man_en[0] 0: Window size from window top 1: Window size from register
0x5C09	PX CNT	–	R	Bit[7:5]: Not used Bit[4:0]: px_cnt[12:8] Pixel count from input image in horizontal
0x5C0A	PX CNT	–	R	Bit[7:0]: px_cnt[7:0] Pixel count from input image in horizontal
0x5C0B	LN CNT	–	R	Bit[7:4]: Not used Bit[3:0]: ln_cnt[11:8] Line count from input image in vertical
0x5C0C	LN CNT	–	R	Bit[7:0]: ln_cnt[7:0] Line count from input image in vertical
0x5C80~ 0x5C8D	RSVD	–	–	Reserved
0x5CA0~ 0x5CA6	RSVD	–	–	Reserved
0x5C90~ 0x5C97	RSVD	–	–	Reserved

6.34 OTP control [0x5C80 - 0x5C8D, 0x5CA0 - 0x5CA6, 0x5C90 - 0x5C97]

table 6-34 OTP control registers (sheet 1 of 2)

address	register name	default value	R/W	description
0x5C80	START ADDR	0x00	RW	Bit[7:5]: Not used Bit[4:0]: start_addr[12:8]
0x5C81	START ADDR	0x00	RW	Bit[7:0]: start_addr[7:0]
0x5C82	END ADDR	0x09	RW	Bit[7:5]: Not used Bit[4:0]: end_addr[12:8]
0x5C83	END ADDR	0xFF	RW	Bit[7:0]: end_addr[7:0]
0x5C84	R CTRL04	0x02	RW	Bit[7]: Debug mode Bit[6]: bin_cluster_sel Bit[5]: Debug mode Bit[4]: man_inc_en Bit[3]: disable_mf Bit[2]: disable_offset Bit[1]: mirror_opt Bit[0]: disable_bin
0x5C85	R CTRL05	0x6C	RW	Bit[7]: Debug mode Bit[6:5]: recov_method Bit[4:3]: Debug mode Bit[2]: flip_opt Bit[1]: expo_en Bit[0]: gain_en
0x5C86	EXPO CONSTRAIN	0x00	RW	Bit[7]: Not used Bit[6:0]: expo_constrain[14:8]
0x5C87	EXPO CONSTRAIN	0x00	RW	Bit[7:0]: expo_constrain[7:0]
0x5C88	GAIN CONSTRAIN	0x07	RW	Bit[7:6]: Not used Bit[5:0]: gain_constrain[5:0]
0x5C89	R CTRL09	0x48	RW	Bit[7]: xy_end_sel Bit[6]: vsync_rst_en Bit[5]: Debug mode Bit[4]: thre_en Bit[3:0]: Thre
0x5C8A	MAN X EVEN INC	0x01	RW	Bit[7:5]: Not used Bit[4:0]: man_x_even_inc[4:0]
0x5C8B	MAN X ODD INC	0x01	RW	Bit[7:5]: Not used Bit[4:0]: man_x_odd_inc[4:0]
0x5C8C	MAN Y EVEN INC	0x01	RW	Bit[7:5]: Not used Bit[4:0]: man_y_even_inc[4:0]

table 6-34 OTP control registers (sheet 2 of 2)

address	register name	default value	R/W	description
0x5C8D	MAN Y ODD INC	0x01	RW	Bit[7:5]: Not used Bit[4:0]: man_y_odd_inc[4:0]
0x5CA0	MAN X OFFSET	0x00	RW	Bit[7:5]: Not used Bit[4:0]: man_x_offset[12:8]
0x5CA1	MAN X OFFSET	0x00	RW	Bit[7:0]: man_x_offset[7:0]
0x5CA2	MAN Y OFFSET	0x00	RW	Bit[7:4]: Not used Bit[3:0]: man_y_offset[11:8]
0x5CA3	MAN Y OFFSET	0x00	RW	Bit[7:0]: man_y_offset[7:0]
0x5CA4	END ADDR BIN	0x00	RW	Bit[7:5]: Not used Bit[4:0]: end_addr_bin[12:8]
0x5CA5	END ADDR BIN	0x00	RW	Bit[7:0]: end_addr_bin[7:0]
0x5CA6	R CTRL26	0x00	RW	Bit[7]: y_bin_man_en Bit[6]: y_bin4_man Bit[5]: y_bin3_man Bit[4]: y_bin2_man Bit[3]: x_bin_man_en Bit[2]: x_bin4_man Bit[1]: x_bin3_man Bit[0]: x_bin2_man
0x5C90	X OFFSET	–	R	Bit[7:5]: Not used Bit[4:0]: x_offset[12:8]
0x5C91	X OFFSET	–	R	Bit[7:0]: x_offset[7:0]
0x5C92	Y OFFSET	–	R	Bit[7:4]: Not used Bit[3:0]: y_offset[11:8]
0x5C93	Y OFFSET	–	R	Bit[7:0]: y_offset[7:0]
0x5C94	X EVEN INC	–	R	Bit[7:5]: Not used Bit[4:0]: x_even_inc[4:0]
0x5C95	X ODD INC	–	R	Bit[7:5]: Not used Bit[4:0]: x_odd_inc[4:0]
0x5C96	Y EVEN INC	–	R	Bit[7:5]: Not used Bit[4:0]: y_even_inc[4:0]
0x5C97	Y ODD INC	–	R	Bit[7:5]: Not used Bit[4:0]: y_odd_inc[4:0]

7 operating specifications

7.1 absolute maximum ratings

table 7-1 absolute maximum ratings

parameter		absolute maximum rating[a]
ambient storage temperature		-40°C to +125°C
supply voltage (with respect to ground)	V_{DD-A}	4.5V
	V_{DD-D}	1.8V
	V_{DD-IO}	4.5V
electro-static discharge (ESD)	human body model	2000V
	machine model	200V
all input/output voltages (with respect to ground)		-0.3V to V_{DD-IO} + 1V
I/O current on any input or output pin		± 200 mA

a. exceeding the absolute maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

7.2 functional temperature

table 7-2 functional temperature

parameter	range
operating temperature (for applications up to 24 fps)[a]	-30°C to +85°C junction temperature
stable image temperature[b]	0°C to +60°C junction temperature

a. sensor functions but image quality may be noticeably different at temperatures outside of stable image range

b. image quality remains stable throughout this temperature range

7.3 DC characteristics

table 7-3 DC characteristics (-30°C < T_J < 85°C)

symbol	parameter	min	typ	max	unit
supply					
V_{DD-A}	supply voltage (analog)	2.7	2.8	3.0	V
V_{DD-D}	supply voltage (digital core)	1.1	1.2	1.3	V
V_{DD-IO}	supply voltage (digital I/O)	1.7	1.8	1.9	V
I_{DD-A}			49		mA
I_{DD-D}[a]	active (operating) current		144		mA
I_{DD-IO}			2		mA
$I_{DDS-SCCB}$			6000		µA
$I_{DDS-PWDN}$	standby current[b]		6000		µA
$I_{DDS-XSHUTDN}$			3		µA
digital inputs (typical conditions: AVDD = 2.8V, DVDD = 1.2V, DOVDD = 1.8V, EVDD = 1.2V)					
V_{IL}	input voltage LOW			0.54	V
V_{IH}	input voltage HIGH	1.26			V
C_{IN}	input capacitor			10	pF
digital outputs (standard loading 25 pF)					
V_{OH}	output voltage HIGH	1.62			V
V_{OL}	output voltage LOW			0.18	V
serial interface inputs					
V_{IL}[c]	SCL and SDA	-0.5	0	0.54	V
V_{IH}	SCL and SDA	1.28	1.8	3.0	V

a. I_{DD-D} (DVDD) is based on DPC off

b. standby current is measured at room temperature

c. based on DOVDD = 1.8V

7.4 timing characteristics

table 7-4 timing characteristics

symbol	parameter	min	typ	max	unit
oscillator and clock input					
f_{OSC}	frequency (XVCLK)[a]	6	24	64	MHz
t_r, t_f	clock input rise/fall time			(see footnote [b])	ns
	clock input duty cycle	45	50	55	%

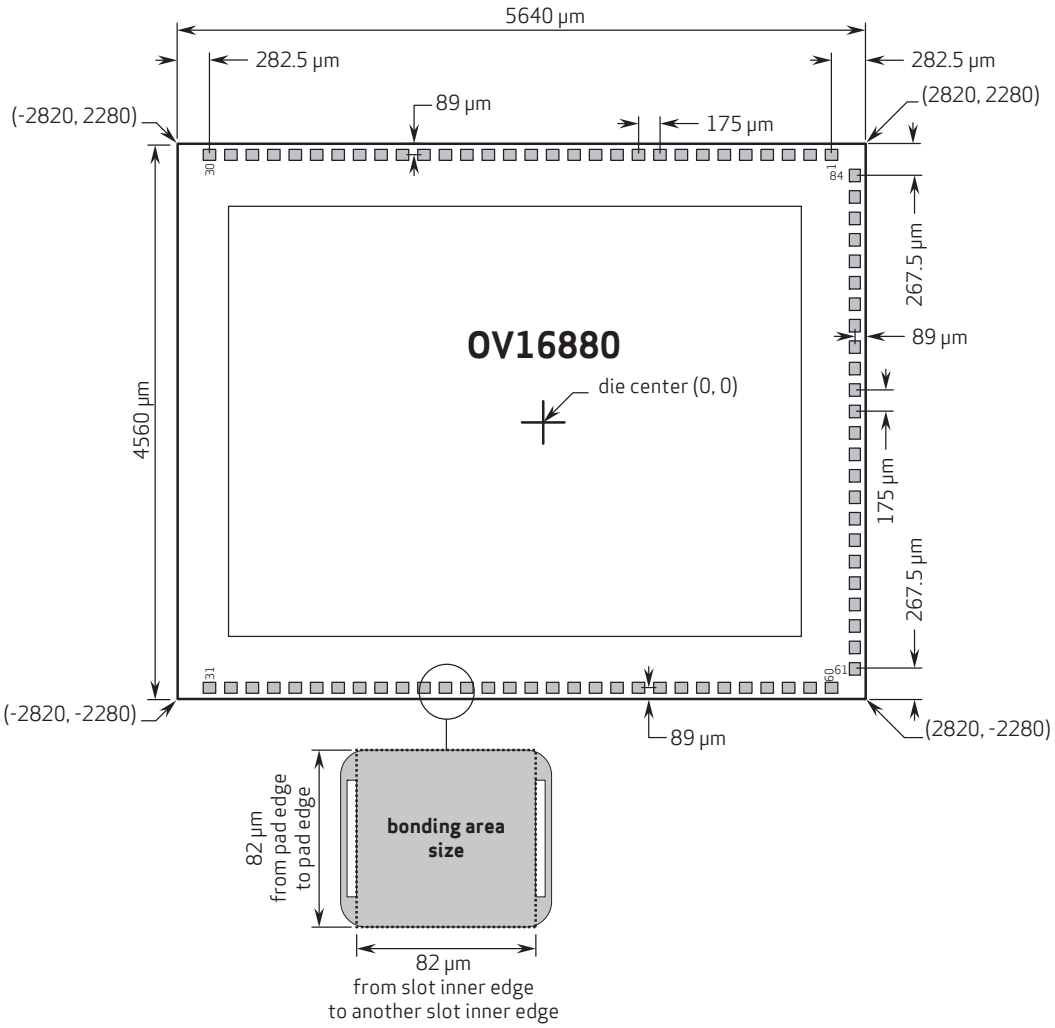
a. for input clock range 6~64MHz, the OV16880 can tolerate input clock period jitter up to 600ps peak-to-peak

b. for clock input rise/fall time, max is 27% of whole clock period

8 mechanical specifications

8.1 COB physical specifications

figure 8-1 COB die specifications



note 1 all dimensions and coordinates are in µm unless otherwise specified.

note 2 bonding outside the defined area is prohibited as it may cause failue in reliability or functionality 16880_COB_DS_8_1

table 8-1 pad location coordinates (sheet 1 of 3)

pad number	pad name	x coordinate	y coordinate	bonding area size
1	DOGND	2537.5	2191	82x82
2	ADVDD	2362.5	2191	82x82
3	ADVDD	2187.5	2191	82x82
4	AGND	2012.5	2191	82x82
5	AGND	1837.5	2191	82x82
6	AVDD	1662.5	2191	82x82
7	AVDD	1487.5	2191	82x82
8	DOGND	1312.5	2191	82x82
9	GPIO0	1137.5	2191	82x82
10	GPIO1	962.5	2191	82x82
11	GPIO2	787.5	2191	82x82
12	GPIO3	612.5	2191	82x82
13	DOVDD	437.5	2191	82x82
14	AGND	262.5	2191	82x82
15	AGND	87.5	2191	82x82
16	PIXVDD	-87.5	2191	82x82
17	PIXVDD	-262.5	2191	82x82
18	AGND	-437.5	2191	82x82
19	AGND	-612.5	2191	82x82
20	AVDD	-787.5	2191	82x82
21	DOGND	-962.5	2191	82x82
22	ATEST	-1137.5	2191	82x82
23	AVDD	-1312.5	2191	82x82
24	AVDD	-1487.5	2191	82x82
25	AGND	-1662.5	2191	82x82
26	AGND	-1837.5	2191	82x82
27	ADVDD	-2012.5	2191	82x82
28	ADVDD	-2187.5	2191	82x82
29	DOGND	-2362.5	2191	82x82
30	DVDD	-2537.5	2191	82x82

table 8-1 pad location coordinates (sheet 2 of 3)

pad number	pad name	x coordinate	y coordinate	bonding area size
31	AGND	-2537.5	-2191	82x82
32	AGND	-2362.5	-2191	82x82
33	AVDD	-2187.5	-2191	82x82
34	VH1	-2012.5	-2191	82x82
35	VN2	-1837.5	-2191	82x82
36	VN1	-1662.5	-2191	82x82
37	DOGND	-1487.5	-2191	82x82
38	DVDD	-1312.5	-2191	82x82
39	DOVDD	-1137.5	-2191	82x82
40	DOGND	-962.5	-2191	82x82
41	DVDD	-787.5	-2191	82x82
42	MDP2	-612.5	-2191	82x82
43	MDN2	-437.5	-2191	82x82
44	EVDD	-262.5	-2191	82x82
45	MDP0	-87.5	-2191	82x82
46	MDN0	87.5	-2191	82x82
47	PVDD	262.5	-2191	82x82
48	EGND	437.5	-2191	82x82
49	DOGND	612.5	-2191	82x82
50	DVDD	787.5	-2191	82x82
51	LVDD	962.5	-2191	82x82
52	MCP	1137.5	-2191	82x82
53	MCN	1312.5	-2191	82x82
54	EGND	1487.5	-2191	82x82
55	MDP1	1662.5	-2191	82x82
56	MDN1	1837.5	-2191	82x82
57	EVDD	2012.5	-2191	82x82
58	MDP3	2187.5	-2191	82x82
59	MDN3	2362.5	-2191	82x82
60	DOGND	2537.5	-2191	82x82

table 8-1 pad location coordinates (sheet 3 of 3)

pad number	pad name	x coordinate	y coordinate	bonding area size
61	FREX	2731	-2012.5	82x82
62	ILPWM	2731	-1837.5	82x82
63	SID	2731	-1662.5	82x82
64	XVCLK	2731	-1487.5	82x82
65	DVDD	2731	-1312.5	82x82
66	DOGND	2731	-1137.5	82x82
67	PWDNB	2731	-962.5	82x82
68	XSHUTDN	2731	-787.5	82x82
69	DOVDD	2731	-612.5	82x82
70	DVDD	2731	-437.5	82x82
71	DOGND	2731	-262.5	82x82
72	SDA	2731	-87.5	82x82
73	SCL	2731	87.5	82x82
74	HREF	2731	262.5	82x82
75	VSYNC	2731	437.5	82x82
76	STROBE	2731	612.5	82x82
77	DVDD	2731	787.5	82x82
78	DOGND	2731	962.5	82x82
79	GPIO4	2731	1137.5	82x82
80	DOVDD	2731	1312.5	82x82
81	DOGND	2731	1487.5	82x82
82	DVDD	2731	1662.5	82x82
83	FSIN	2731	1837.5	82x82
84	TM	2731	2012.5	82x82

8.2 reconstructed wafer (RW) physical specifications

- maximum total die count: 919
- film frame: Compact Disco Stainless SUS420
- carrier tape: UV tape

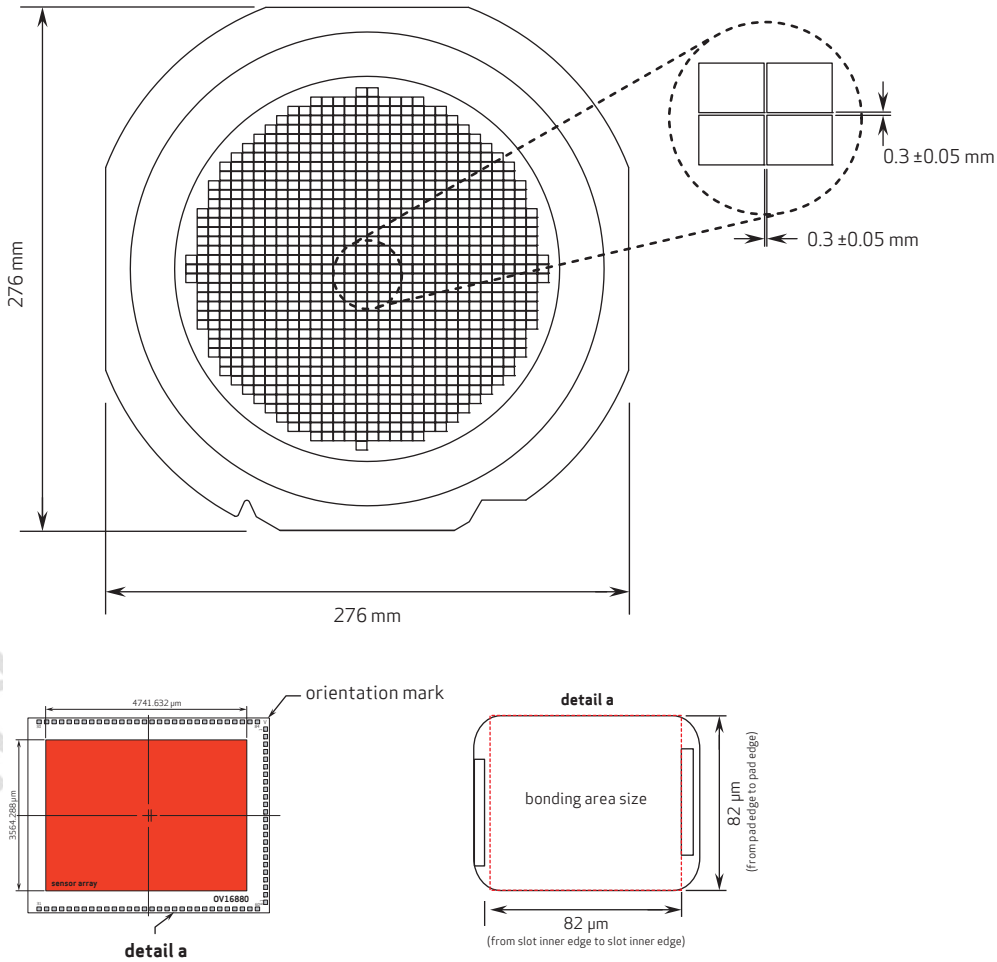
table 8-2 RW physical dimensions

feature	dimensions
RW physical dimensions	8" RW on 12" frame
wafer thickness (OVXXXXX-ABCD)	
C=5	150 µm ± 10 µm (5.9 mil ± 0.4 mil)
reconstructed wafer street width	300 µm ± 50 µm (11.8 mil ± 2 mil)
placement accuracy x, y, theta	± 50 µm (± 2 mil), <1.0 degree
singulated die size	
width	5690 µm ± 20 µm (224.0 mil ± 0.8 mil)
length	4610 µm ± 20 µm (181.5mil ± 0.8 mil)
bond pad size	104 µm × 85 µm (4.1 mil × 3.3mil)
minimum bond pad pitch	175 µm (6.9 mil)
bonding area size	82 µm × 82 µm (3.2 mil × 3.2 mil)
optical array	
die center	(0, 0)
optical center from die center[a]	(45, 0)

a. based on die orientation on frame with notch facing down position

note
Actual die count varies and the absent die may be less than 10% of the maximum total die count (excluding the last frame of the wafer lot).

figure 8-2 OV16880 RW physical diagram



note 1 bonding outside the defined bonding area is prohibited, it may potentially induce reliablity issues or functionality failure

note 2 keep-out-of-contact areas are highlighted in red color for related process fixtures/tools (e.g., nozzle, collets, etc.)

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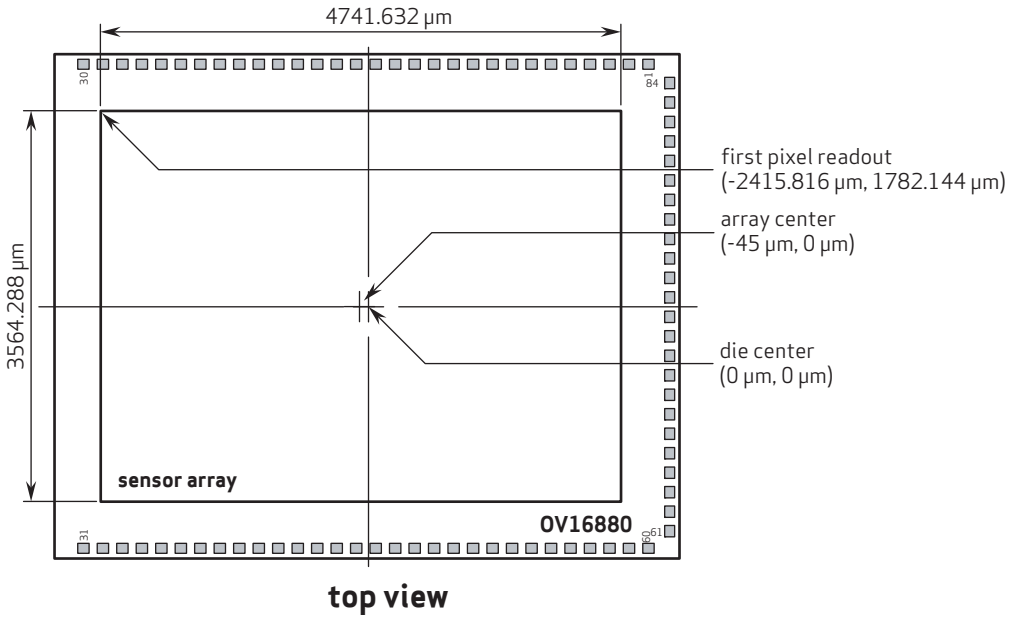
9 optical specifications

9.1 sensor array center

figure 9-1 sensor array center



note 1 this drawing is not to scale and is for reference only.

note 2 as most optical assemblies invert and mirror the image, the chip is typically mounted with pad 1 oriented down on the PCB.

16880_COB_DS_9_1

9.2 lens chief ray angle (CRA)

figure 9-2 chief ray angle (CRA)

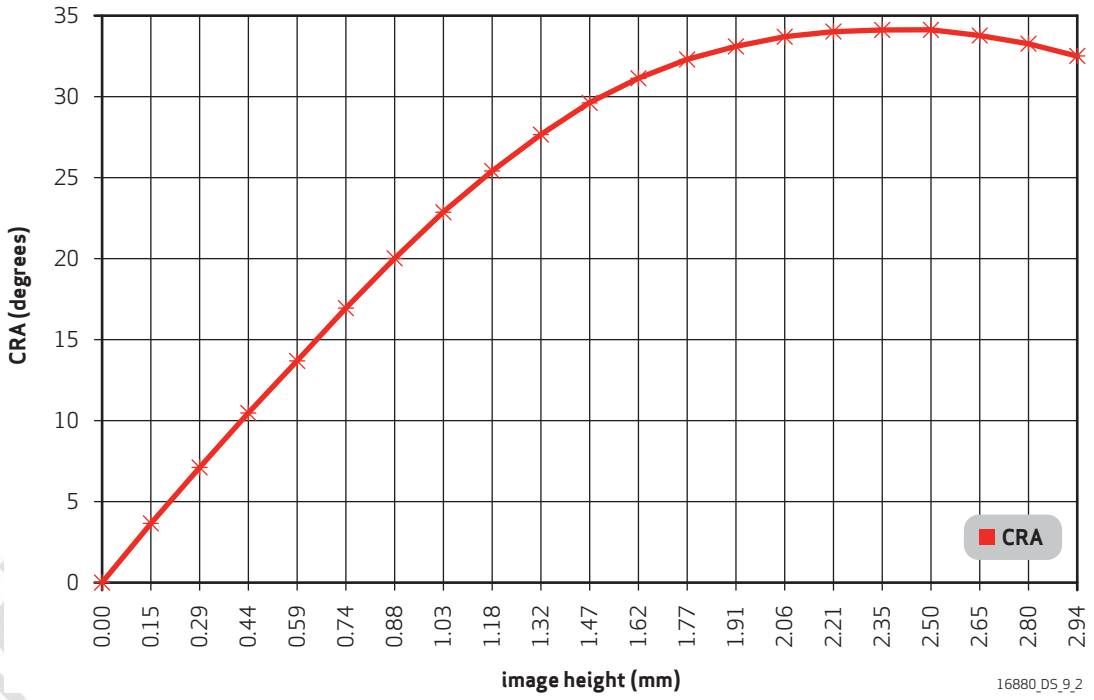


table 9-1 CRA versus image height plot (sheet 1 of 2)

field (%)	image height (mm)	CRA (degrees)
0.00	0.00	0.00
0.05	0.15	3.59
0.10	0.29	7.05
0.15	0.44	10.45
0.20	0.59	13.77
0.25	0.74	16.99
0.30	0.88	20.05
0.35	1.03	22.90
0.40	1.18	25.46
0.45	1.32	27.71

table 9-1 CRA versus image height plot (sheet 2 of 2)

field (%)	image height (mm)	CRA (degrees)
0.50	1.47	29.60
0.55	1.62	31.14
0.60	1.77	32.34
0.65	1.91	33.19
0.70	2.06	33.76
0.75	2.21	34.08
0.80	2.35	34.20
0.85	2.50	34.14
0.90	2.65	33.89
0.95	2.80	33.42
1.00	2.94	32.63

appendix A handling of RW devices

A.1 ESD /EOS prevention

1. Ensure that there is 500V ESD control in all work areas.
2. Use ESD safety shoes, ground strap, and static control smocks in test areas.
3. Use grounded work carts and tables in inspection areas.
4. OmniVision recommends the use of ionized air in all work areas.

A.2 particles and cleanliness of environment

1. All production, inspection and packaging areas should meet Class10 environment requirements.
2. Use optical microscopes with 50X and 100X magnifications for particle inspection.
3. Ensure that there is good cassette sealing for particle protection during storage.
4. OmniVision recommends water cleaning to remove removable particles.
5. RW die should be stored in nitrogen gas purged cabinets with temperature less than 30°C and relative humidity of 60% before assembly.

A.3 other requirements

1. Reliability assurance of RW or COB bare die is certified by product reliability of the bare die in a CLCC, CSP or QFP package form factor. Precautions should be taken if the packaging form factor of the bare die is other than these specified.
2. Avoid exposure to strong sunlight for extended periods of time as the color filter of the image sensor may become discolored.
3. Avoid direct exposure of the sensor bare die to high temperature and/or humidity environment as sensor characteristics will be affected. Extra precautions should be exercised if the bare die experiences temperatures exceeding 260°C for more than 75 seconds.

revision history

version 1.0 09.04.2015

- initial release

version 1.01 09.15.2015

- in chapter 4, updated table 4-1
- in table 4-4, changed description of register bit 0x4000[6] to Bit[6]: Vertical flip black lines, 0: Normal, 1: Vertical flip
- in chapter 5, updated figure 5-3
- in table 6-16, changed description of register bit 0x4000[6] to Bit[6]: Vertical flip black lines, 0: Normal, 1: Vertical flip

version 1.1 12.18.2015

- in key specifications, changed active power requirements to 300mW, standby power requirements to 6mA, XSHUTDN power requirements to 3µA, sensitivity to 3200 e^-/Lux-sec, max S/N ratio to 36.8 dB, dynamic range to 72 dB @ 16x gain, dark current to 4e^-/sec @ 60°C junction temperature and removed maximum exposure interval specification
- in section 2.6.2, changed first sentence to "To avoid bad frames, OmniVision recommends using group hold..." and changed second sentence to "To set the sensor into hardware power down mode, pull XSHUTDN signal low."
- in section 2.10, updated second paragraph and added figure 2-7
- in section 3.6, updated first paragraph and removed all other subsections
- in section 3.7, updated first paragraph
- in chapter 3, added section 3.8 including figures 3-7 and 3-8
- in section 4.5, added table 4-5
- in chapter 5, removed section 5.3
- in section 5.4 (previously section 5.5), corrected grammar in first three paragraphs
- in section 5.5 (previously section 5.6), changed first two sentences to "The main purpose of the DPC function is to remove white and black defective pixels. If the pixel is defective, DPC will..."
- in section 5.7 (previously section 5.8), updated second, third and fourth paragraphs
- in section 5.8 (previously section 5.9), corrected grammar
- in section 6.13, changed title to OTP control and changed table 6-13 title to OTP control registers
- in table 7-3, removed TBDs for min and max values of I_{DD-A}, I_{DD-D}, I_{DD-IO}, $I_{DDS-SCCB}$, $I_{DDS-PWDN}$, and $I_{DDS-XSHUTDN}$
- in table 7-3, changed typ values of I_{DD-A}, I_{DD-D}, I_{DD-IO}, $I_{DDS-SCCB}$, $I_{DDS-PWDN}$, and $I_{DDS-XSHUTDN}$ to 49 mA, 144 mA, 2mA, 6000µA, 6000µA, and 3µA, respectively and added table footnote c

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- in table 4-1, changed description of register bit 0x3821[2] to Bit[2]: Horizontal mirror control, 0: Mirrored image, 1: Normal image
- in table 6-8, changed description of register bit 0x3821[2] to Bit[2]: Horizontal mirror control, 0: Mirrored image, 1: Normal image

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