MT6370 Power Management IC
Product Brief

Version: **1.0**
Release date: **2023-09-18**

The full datasheet is available with an NDA

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Version History

Version	Date	Description
1.0	2023-09-18	Official release

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1 Overview

1.1 Features

- **Battery Charger**
  - High-Accuracy Voltage/Current Regulation
  - Average Input Current Regulation (AICR) : 0.1A to 3.25A in 50mA steps
  - Charge Current Regulation Accuracy : ±7%
  - Charge Voltage Regulation Accuracy : ±0.5% (0 to 70°C)
  - Battery Temperature Sensing
  - Synchronous 1.5Mz Frequency PWM Controller with Up to 95% Duty Cycle
  - Thermal Regulation and Protection
  - Over-Temperature Protection
  - Input Over-Voltage Protection
  - IRQ Output for Communication via I^2C
  - Automatic Charging
  - BATFET Control to Support Ship Mode, Wake Up, and Full System Reset
  - Resistance Compensation from Charger Output to Cell Terminal
  - USB OTG Output Voltage Range : 4.425V to 5.825V
  - D+/D- Detection for BC1.2
  - Integrated ADCs for System Monitoring (Charger Current, Voltage, and Temperature)
  - JEITA Thermal Comparator Accuracy ±1% VTS
  - Low Battery Protection from 2.3V to 3.8V for Boost Operation
  - Initial VOREG Set for Relieve Battery Protection
  - External OVP MOSFET Driving for Higher Surge Application, Up to AMR 28V
- **USB_PD**
  - PD-Compatible Dual-Role
  - Attach/Detach Detection as Host, Device or Dual-Role Port
  - Current Capability Definition and Detection
  - Cable Recognition
  - Alternate Mode Supported
  - Supports VCONN with Programmable Over-Current Protection (OCP)
  - Dead Battery Support
  - Ultra-Low Power Mode for Attach Detection (<10mA)
  - BIST Mode Supported
  - USB PD3.0
- **Backlight WLED Driver**
  - Drives up to 4 Strings of 8 series WLEDs
  - External PWM Pin and I2C-Controlled with Programmable 11 bits of Linear and Exponential Brightness
  - I2C-Programmable Over-Voltage Protection (OVP) Threshold
  - Supports Torch Mode and Strobe Mode for Front Cameras

  - Auto Switch Frequency Mode (500kHz, 1MHz)
  - Four Over-Voltage Protection Thresholds (17V, 21V, 25V, and 29V)
  - Four Over-Current Protection Thresholds (900mA, 1200mA, 1500mA, and 1800mA)
  - Front-Facing Flash with 300% Brightness for Selfshot
- **Flash LED Driver**
  - Synchronous Boost Dual Flash LED Driver with Dual Independently-Programmable LED Current Sources
  - Torch Mode Current : from 25mA to 400mA in 12.5mA Steps per Channel
  - I^2C-Programmable Flash Safety Timer, from 64ms to 2432ms with 32ms/Step
  - Flash LED1/LED2 Short-Circuit Protection, and Output Short-Circuit Protection
  - TXMask Protection with dedicated FL_TXMASK Pin
  - Shared Charger/OTG as Power Stage
  - Independent Torch Bypass MOSFET from VSYS
  - Strobe Mode Current : 50mA to 1.5A in 12.5mA Steps or 25mA to 750mA in 6.25mA Steps per Channel, and Up to 2.5A in Total
- **Display Bias Driver**
  - I2C-Programmable Output Voltages
  - Flexible Output Voltages (VDB_BST, VDB_POS, VDB_NEG) Setting
  - Boost Converter Output Voltage (VDB_BST) Range : 4V to 6.2V, 50mV/Step
  - Positive Voltage Output (VDB_POS) Range : 4V to 6V, 50mV/Step
  - Negative Voltage Output (VDB_NEG) Range : -4V to -6V, 50mV/Step
  - Selectable Output Mode (Fast Discharge or Float) when Positive/Negative Voltage Output Disabled
  - External Independent Positive/Negative Enable Control
  - True Load Disconnect, Over-Current Protection, and Positive/Negative Short-Circuit Protection Function
  - Output Current : 80mA
  - Power-Saving by Periodic Mode
- **LDO**
  - Output Voltage Range : 1.6V to 4V, 200mV/Step
  - Output Current : 400mA
  - High PSRR and Low Dropout LDO
- **RGB LED Driver**
  - 4-Channel LED Driver
  - Sink Current for 3 RGB LEDs : 24mA/Channel in 4mA Steps
  - PWM Dimming Frequency Range : 0.1Hz to 1kHz
  - RGB_ISINK4 for CHG_VIN Power Good Indicator
  - Support Register Mode, PWM Mode, and Breath Mode

1.2 Applications

- Cellular Telephones
- Personal Information Appliances
- Tablet PCs
- Portable Instruments
- Industrial HMI, desktop POS, KIOSK, digital signage

1.3 General Descriptions

The MT6370 is a highly-integrated smart power management IC, which includes a single cell Li-Ion/Li-Polymer switching battery charger, a USB Type-C & Power Delivery (PD) controller, dual Flash LED current sources, a RGB LED driver, a backlight WLED driver, a display bias driver and a general LDO for portable devices.

The switching charger integrates a synchronous PWM controller, power MOSFETs, input current sensing and input current regulation, high-accuracy voltage regulation, and charge termination circuitry. Besides, the charge current is regulated through the integrated sensing resistors. It also features USB On-The-Go (OTG) support.

The USB Type-C & PD controller complies with the latest USB Type-C and PD standards. It integrates a complete Type-C transceiver including the Type-C termination resistors, Rp and Rd, and enables the USB Type-C detection including attach and orientation. It also integrates the physical layer of the USB BMC power delivery protocol, allowing power transfers and role swaps. The BMC PD function provides full support for alternate modes on the USB Type-C standard.

Dual independent current sources supply for each flash LED. The power for the current sources in strobe mode are from the CHG_VMID pin, which is supplied from the charger in reverse boost mode, the same operation as OTG mode of the charger. The high-side current sources, allowing for grounded-cathode connection for LEDs, provide strobe mode current levels from 25mA to 1.5A in a 12.5 mA step or from 25mA to 750mA in a 6.25mA step and torch mode current levels from 25mA to 400mA in a 12.5mA step. The two channels can support totally up to 2.5A.

The backlight WLED driver supports up to a 29V output voltage for 4 channels of 8 series WLEDs. Each channel supports up to 30mA of current capability with 2048 current steps in exponential or linear mapping curves. The backlight brightness is controlled by the I^2C interface and an external PWM control. The PWM frequency range is from 50Hz to 50kHz. The MT6370 can also support torch/strobe backlight modes with regulated constant current for front camera screen flash applications.

The display bias driver (DB) is implemented with a single-inductor boost and an inverting charge pump to achieve a smaller PCB area, compared with a dual-inductor boost converter. The display bias driver is used to provide a negative voltage output (VDB_NEG) through the DB_NEGVOUT pin and a positive voltage output (VDB_POS) through the DB_POSVOUT pin. The negative voltage output comes from the boost converter output voltage (VDB_BST) at the DB_BSTVOUT pin, and the positive voltage output is from the DB_POSVOUT voltage passing through an LDO to reduce power noise. The VDB_POS and VDB_NEG voltage ranges can be programmed from 4V to 6V and from -4V to -6V with a resolution of 50mV, respectively. These two output rails, usually connected to a Source Driver IC, can support up to 50mA output current capability to drive up to 10" TFT-LCD panels.

The LDO can be used to supply power to an Eccentric Rotating Mass (ERM) Motor in mobile phones and other hand-held devices. The output voltage is programmable in the range of 1.6V to 4V via the I^2C interface.

The RGB LED driver is a 4-Channel smart LED string controller to drive 3 channels of LEDs with a sink current of up to 24mA and a CHG_VIN power good indicator with a sink current of up to 6mA. All channels can be set independently via the I^2C interface, and are provided with three operation modes: Register Mode, PWM Mode and Breath Mode.

The MT6370 is available in a WL-CSP-93B 4.22x4.32 (BSC) package.

1.4 Ordering Information

MT6370 □
└Package Type
P : WL-CSP-93B 4.22x4.32 (BSC)

Figure 1-1. Ordering information

1.5 Pin Assignments and Descriptions

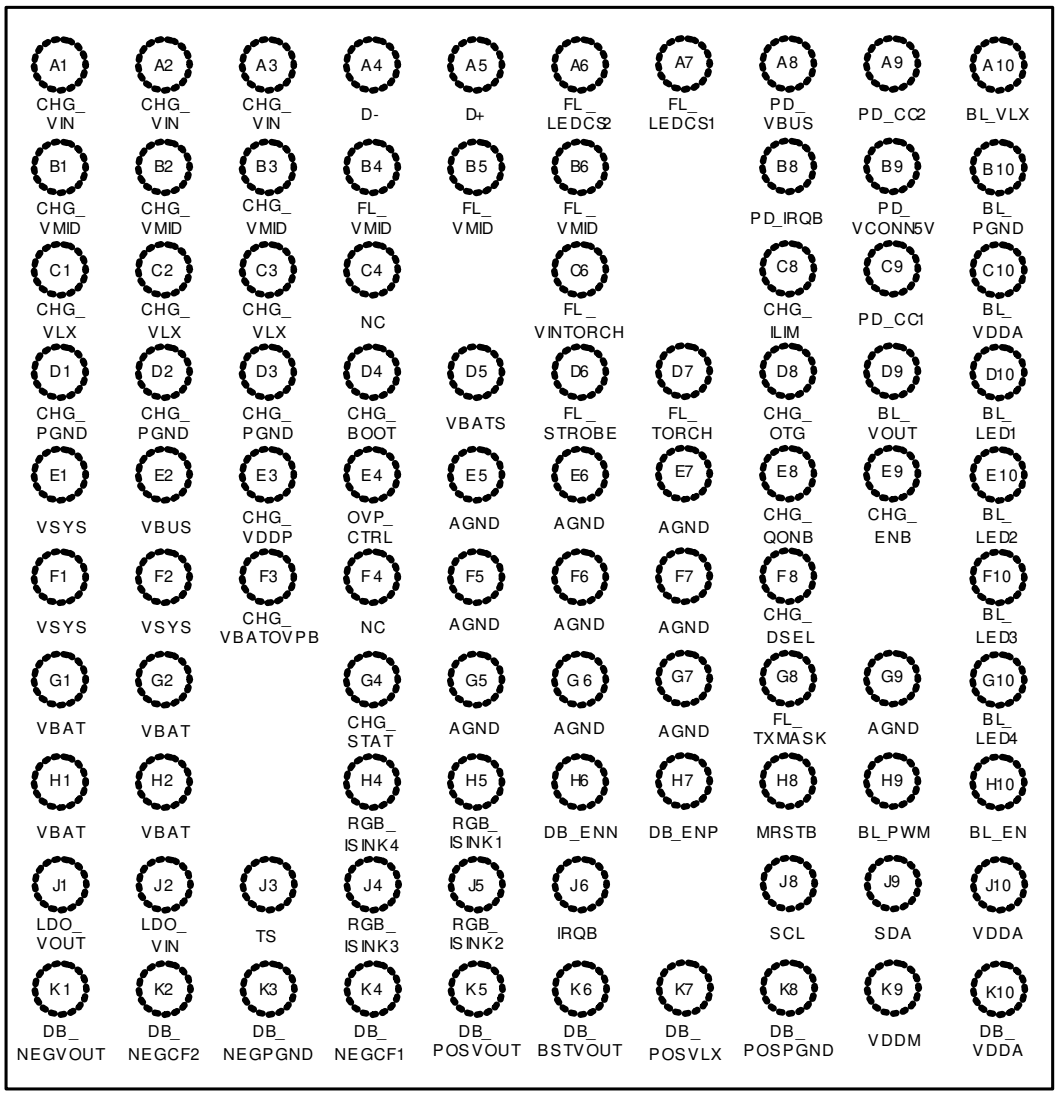


Figure 1-2. MT6370 WL-CSP-93B 4.22x4.32 (BSC) (top view)

Table 1-1. MT6370 pin descriptions

Pin No.	Pin Name	Pin Description
A1, A2, A3	CHG_VIN	Charger power input.
A4	D-	USB D- port.
A5	D+	USB D+ port.
A6	FL_LEDCS2	High-side current source output 2 for flash LED2.
A7	FL_LEDCS1	High-side current source output 1 for flash LED1.
A8	PD_VBUS	VBUS input for attach and detach detection when the device operates as an UFP port.
A9	PD_CC2	Type-C connector Configuration Channel (CC) 2, used to detect a cable plug event and determine the cable orientation.
A10	BL_VLX	Backlight boost converter switch node. Connect a 10µH inductor between BL_VLX and VSYS.
B1, B2, B3	CHG_VMID	Connection point between the reverse-blocking MOSFET and the high-side switching MOSFET.
B4, B5, B6	FL_VMID	Flash LED driver power input for strobe mode. Connect a 4.7µF ceramic capacitor between FL_VMID and ground.
B8	PD_IRQB	Interrupt output, active-low open-drain, to request the processor to check the registers.
B9	PD_VCONN5V	Regulated input voltage to power PD_CC pins as VCONN.
B10	BL_PGND	Backlight ground. Tie BL_PGND and ground on the PCB.
C1, C2, C3	CHG_VLX	Charger switch node for output inductor connection.
C4	NC	No internal connection.
C6	FL_VINTORCH	Flash LED driver power input for torch mode.
C8	CHG_ILIM	Input current limit setting pin. A resistor is connected from CHG_ILIM pin to ground to set the maximum input current limit. The actual input current limit is the lower value set through the CHG_ILIM pin and IAICR register bits.
C9	PD_CC1	Type-C connector Configuration Channel (CC) 1, used to detect a cable plug event and determine the cable orientation.
C10	BL_VDDA	Backlight analog power supply. Connect a 1µF ceramic capacitor between BL_VDDA and ground.
D1, D2, D3	CHG_PGND	Charger ground. Tie CHG_PGND and ground on the PCB.
D4	CHG_BOOT	Charger bootstrap voltage to supply the high-side MOSFET gate driver. Connect a capacitor between CHG_BOOT and CHG_VLX.
D5	VBATS	Battery voltage-sense input.
D6	FL_STROBE	Flash LED Strobe mode enable input.
D7	FL_TORCH	Flash LED Torch mode enable input.
D8	CHG_OTG	OTG boost mode enable control, active-high. Act with OTG_Pin_EN (0x11[1]).
D9	BL_VOUT	Backlight output voltage.
D10	BL_LED1	Backlight current regulator output 1.
E1, F1, F2	VSYS	System connection node. Internal BATFET is connected between VSYS and VBAT. Connect a 22µF ceramic capacitor between VSYS and ground.
E2	VBUS	VBUS input voltage for over-voltage protection detection.
E3	CHG_VDDP	Regulated output voltage to supply for the PWM low-side gate driver and the bootstrap capacitor. Connect a 1µF ceramic capacitor CHG_VDDP to ground. 1. If VBUS is plugged in, CHG_VDDP will be powered by VBUS and regulated to 4.9V. 2. If VBUS is unplugged, the charger will operate in sleep mode and the CHG_VDDP voltage will be 0V. * For 2. : Since the CHG_VDDP voltage is also used to power the TS resistor, when the charger is in sleep mode, the CHG_VDDP will be woken up (be

Pin No.	Pin Name	Pin Description
		reactivated) if VBAT is greater than forward voltage (VF) of the internal high-side (HS) MOS diode by VSLEEP_EXIT with all function of the internal ADC being activated. The CHG_VDDP wake-up time is 500ms.
E4	OVP_CTRL	Input over-voltage protection (IN_OVP) control input.
E5, E6, E7, F5, F6, F7, G5, G6, G7, G9	AGND	Analog ground. Tie AGND and ground on the PCB.
E8	CHG_QONB	Internal BATFET enable control input. In shipping mode, CHG_QONB is pulled Low for the duration of tSHIPMODE_CHG (typical 0.9s) to exit shipping mode.
E9	CHG_ENB	Charger enable input, active-low.
E10	BL_LED2	Backlight current regulator output 2.
F3	CHG_VBATOVPB	Battery over-voltage protection (BAT OVP) indication, open–drain and active-low output: Low if BAT OVP occurs, and High, otherwise.
F4	NC	No internal connection.
F8	CHG_DSEL	Open-drain output. When the device starts to detect input power source, CHG_DSEL drives Low to indicate that detection is in progress and the device needs to take control of the D+ and D- signals. When detection is completed, CHG_DSEL holds Low if DCP (Dedicated Charging Port) or HVDCP adapter is detected. CHG_DSEL returns to High if SDP (Standard Downstream Port) or CDP (Charging Downstream Port) is detected.
F10	BL_LED3	Backlight current regulator output 3.
G1, G2, H1, H2	VBAT	Charge current output node for battery connection. The internal BATFET is connected between VSYS and VBAT. Connect a 10µF ceramic capacitor between VBAT and ground.
G4	CHG_STAT	Charge status indication, open-drain output that indicates charge is in progress when held low and charge is finished when held High. If any fault occurs, CHG_STAT will blink at the frequency of 1Hz. Connect a 2.2k to 10kΩ pull-up resistor.
G8	FL_TXMASK	Configurable power amplifier synchronization input or configurable active-high torch mode enable. Connect an internal pull-down resistor of 300kΩ between FL_TXMASK and ground.
G10	BL_LED4	Backlight current regulator output 4.
H4	RGB_ISINK4	RGB LED current sink output 4.
H5	RGB_ISINK1	RGB LED current sink output 1.
H6	DB_ENN	Enable control input for DB_NEGVOUT.
H7	DB_ENP	Enable control input for DB_POSVOUT.
H8	MRSTB	Manual reset input for hardware reset.
H9	BL_PWM	Backlight PWM dimming control input.
H10	BL_EN	Backlight enable control input.
J1	LDO_VOUT	LDO output. Connect a 2.2µF ceramic capacitor between LDO_VOUT and ground.
J2	LDO_VIN	LDO power input. Connect a 2.2µF ceramic capacitor between LDO_VIN and ground.
J3	TS	Battery temperature-sense input, connected to a resistor divider for temperature programming. If there is no need for the battery temperature-sense function, a 50kΩ resistor is connected to CHG_VDDP and another 50kΩ resistor to ground.
J4	RGB_ISINK3	RGB LED current sink output 3.
J5	RGB_ISINK2	RGB LED current sink output 2.
J6	IRQB	Interrupt output, active-low open-drain, to request the processor to read the registers.

Pin No.	Pin Name	Pin Description
J8	SCL	I2C interface serial clock input. Open-drain. An external pull-up resistor is required.
J9	SDA	I2C interface serial data input/output. Open-drain. An external pull-up resistor is required.
J10	VDDA	Regulated power input for an internal analog base. Connect a 1µF ceramic capacitor between VDDA and ground.
K1	DB_NEGVOUT	Display bias negative voltage output from the inverting charge pump. Connect a 10µF ceramic capacitor between DB_NEGVOUT and ground.
K2	DB_NEGCF2	Inverting charge pump connection point for negative terminal of the flying capacitor. Connect a 10µF ceramic capacitor between DB_NEGCF2 and DB_NEGCF1.
K3	DB_NEGPGND	Display bias negative-voltage power ground. Tie DB_NEGPGND and ground on the PCB.
K4	DB_NEGCF1	Inverting charge pump connection point for positive terminal of the flying capacitor. Connect a 10µF ceramic capacitor between DB_NEGCF2 and DB_NEGCF1.
K5	DB_POSVOUT	Display bias positive voltage output from the LDO. Connect a 10µF ceramic capacitor between DB_POSVOUT and ground.
K6	DB_BSTVOUT	Display bias boost converter output. Connect a 10µF ceramic capacitor between DB_BSTVOUT and ground.
K7	DB_POSVLX	Display bias boost converter switch node. Connect a 2.2µH inductor between DB_POSVLX and VSYS.
K8	DB_POSPGND	Display bias positive-voltage power ground. Tie DB_POSPGND and ground on the PCB.
K9	VDDM	Regulated voltage output. Connect a 1µF ceramic capacitor between VDDM and PGND. It also provides power to all VDDA-powered circuits.
K10	DB_VDDA	Display bias analog power supply. Connect a 1µF ceramic capacitor between DB_VDDA and ground.

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

(1)

- BL_VLX, BL_VOUT and (BL_LED1 to BL_LED4) ---------- -0.3V to 30V
- VBUS, PD_VBUS ---------- -0.3V to 28V
- OVP_CTRL, PD_CC1, PD_CC2 ---------- -0.3V to 24V
- CHG_VIN, CHG_VMID, CHG_BOOT, FL_VMID ---------- -0.3V to 22V
- D+, D-, CHG_LX ---------- -0.3V to 16V
  LX (Peak < 100ns duration) ---------- -2V
- DB_POSVOUT, DB_BSTVOUT, DB_POSVLX ---------- -0.3V to 7V
- Negative Charge Pump Switching Voltage (DB_NEGCF2) ---------- 0.3V to -6.5V
- Negative Charge Pump Voltage (DB_NEGVOUT) ---------- 0.3V to -6.5V
- Other Pins ---------- -0.3V to 6V
- Power Dissipation, PD @ T_A = 25°C
  WL-CSP-93B 4.22x4.32 (BSC) ---------- 4.38W
- Package Thermal Resistance (2)
  WL-CSP-93B 4.22x4.32 (BSC), θ_{JA} ---------- 22.8°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- -65°C to 150°C
- ESD Susceptibility (3)
  HBM (Human Body Model) ---------- 2kV

(1) Note 1 Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

(2) Note 2 θ_{JA} is measured under natural convection (still air) at T_A = 25 °C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

(3) Note 3 Devices are ESD sensitive. Handling precaution recommended.

2.2 Recommended Operating Range

(Note)

- VBUS Supply Input Voltage ---------- 4V to 14V
- VBAT Supply Input Voltage ---------- 2.7V to 5.5V
- Junction Temperature Range ---------- 40°C to 125°C
- Ambient Temperature Range ---------- -40°C to 85°C

Note. The device is not guaranteed to function outside its operating conditions.

2.3 Electrical Characteristics

V_{CHG_VIN} = 5V, V_{BAT} = 4.2V, L2 = 1µH, C2 = 2.2µF, C19 = 10µF, T_A = 25°C, unless otherwise specified

Table 2-1. Electrical specifications

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current						
Shutdown Current	I_{SHDN}	On VBAT pin, with all channels shut down, V_{BAT} = 4V	--	60	85	µA
Shipping-Mode Current	I_{BAT_SHIP}	VBAT only, in shipping mode	--	31	46	µA
V_{BUS} Supply Current	I_{VBUS}	V_{CHG_VLX} is non-switching, V_{BUS} = 5V, V_{BAT} = V_{CV_CHG}, ICHG = 0, Flash LED, LDO, Backlight and RGB devices disabled, PD Cable attached (Full functions are not in the communication situation)	--	8.55	11.12	mA
V_{BUS} Supply Current with PD Communication	$I_{VBUS\_PDTX\_ON}$	V_{CHG_VLX} is non-switching, V_{BUS} = 5V, V_{BAT} = V_{CV_CHG}, I_{CHG} = 0, Flash LED, LDO, Backlight and RGB drivers disabled, PD Cable attached (Full functions are in the communication situation)	--	12.55	16.31	mA
V_{BUS} Supply Current with Charger in H-Z Mode	I_{VBUS_HZ}	V_{CHG_VLX} is in high-impedance mode, V_{BUS} = 5V, V_{BAT} = V_{CV_CHG} Flash LED, LDO, Backlight and RGB devices disabled, PD in ultra-low power mode	--	810	1053	µA
BAT Supply Current	$I_{BAT\_LDO\_ON}$	V_{BUS} = 0V, V_{BAT} = 3.8V, charger, Flash LED, Backlight and RGB devices disabled, LDO enabled with load = 0, PD in ultra-low power mode	--	200	300	µA
BAT Supply Current	$I_{BAT\_DB\_ON}$	V_{BUS} = 0V, V_{BAT} = 3.8V, charger, Flash LED, Backlight and RGB devices disabled, display bias driver enabled with load = 0, PD in ultra-low power mode	--	1750	2100	µA
Over-Temperature Protection Threshold	T_{OTP}	Thermal shutdown threshold temperature	--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	Thermal shutdown hysteresis temperature	--	20	--	°C
Control I/O Pin & VDDA						
Logic-Low Threshold Voltage for All Open-Drain Outputs	V_{OL}	I_{DS} = 10mA	--	--	0.4	V
Logic-High Threshold Voltage for All Inputs	V_{IH}	Logic high threshold	1.2	--	--	V
Logic-Low Threshold Voltage for All Inputs	V_{IL}	Logic low threshold	--	--	0.4	V
VDDA Under-Voltage Protection Threshold	V_{VDDA_UVLO}	V_{DDA} falling	2.3	2.4	2.5	V
VDDA Under-Voltage Protection Hysteresis	$V_{VDDA\_UVLO\_HYS}$	V_{DDA} rising	--	0.1	--	V
VDDA Over-Voltage Protection Threshold	V_{VDDA_OVP}	V_{DDA} rising	5.7	5.95	6.2	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VDDA Over-Voltage Protection Hysteresis	$V_{VDDA\_OVP\_HYS}$	V_{DDA} falling	--	0.2	--	V
Pull-Down Resistance on MRSTB	R_{L_MRSTB}		--	300	--	kΩ
OVP Controller						
VBUS POR Threshold for CHG_VIN Only	V_{POR_OVP}	V_{BUS} rising	2.5	2.7	2.9	V
VBUS POR Hysteresis Only for CHG_VIN	$V_{POR\_OVP\_HYS}$	V_{BUS} falling	--	100	--	mV
POR Deglitch Time Only for CHG_VIN	$t_{D\_POR\_OVP}$	V_{BUS} = 5V to 12V	22.4	32	41.6	ms
Over-Voltage Protection Threshold	V_{OVP}	V_{BUS} rising	15.5	16.5	17.5	V
Over-Voltage Protection Hysteresis	V_{OVP_HYS}	V_{BUS} falling	--	200	--	mV
OVP Propagation Delay for MOS Turned Off	t_{PD_OVP}	V_{BUS} from 12V to 20V, (6V/µs), Q_g of MOS at V_{GS} = 4.5V < 20nC	--	0.18	0.25	µs
OVP Recovery Delay	t_{RD_OVP}	V_{BUS} from 20V to 12V	5.6	8	10.4	ms
Charger						
Sleep-Mode Entry Threshold, VBUS-VBAT	$V_{SLEEP\_ENTER\_CHG}$	V_{BUS} falling, 2.5V < V_{BAT} < V_{OREG_CHG}	0	0.04	0.1	V
Sleep-Mode Exit Threshold, VBUS-VBAT	$V_{SLEEP\_EXIT\_CHG}$	V_{BUS} rising, 2.5V < V_{BAT} < V_{OREG_CHG}	0.04	0.1	0.2	V
Sleep-Mode Exit Deglitch Time	$t_{D\_SLEEP\_EXIT\_CHG}$	Exit sleep-mode	--	120	--	ms
CHG_VIN Bad Adapter Threshold	$V_{BAD\_ADP\_CHG}$		--	3.8	--	V
CHG_VIN Bad Adapter Hysteresis	$V_{BAD\_ADP\_HYS\_CHG}$		--	150	--	mV
CHG_VIN Bad Adapter Sink Current	$I_{BAD\_ADP\_SINK\_CHG}$		--	50	--	mA
CHG_VIN Bad Adapter Detection Time	$t_{BAD\_ADP\_DET\_CHG}$		--	30	--	ms
Input Current Limit Factor	K_{ILIM_CHG}	Input current regulation 508mA by ILIM pin with resistance = 698Ω	320	355	390	AΩ
CHG_VIN Minimum Input Voltage Regulation (MIVR) Threshold	V_{MIVR_CHG}	I^2C programmable range in 0.1V steps	3.9	--	13.4	V
CHG_VIN Minimum Input Voltage Regulation Accuracy	$V_{MIVR\_ACC\_CHG}$	V_{MIVR} = 4.4V or 9V	-2	--	2	%
AICR 100mA Mode	$I_{AICR\_100mA\_CHG}$	I_{AICR} = 100mA, V_{CHG_VIN} = 5V, VBAT = 3.8V	86	93	100	mA
AICR 500mA Mode	$I_{AICR\_500mA\_CHG}$	I_{AICR} = 500mA, V_{CHG_VIN} = 5V, VBAT = 3.8V	440	470	500	mA
AICR 1000mA Mode	$I_{AICR\_1000mA\_CHG}$	I_{AICR} = 1000mA, V_{CHG_VIN} = 5V, VBAT = 3.8V	880	940	1000	mA
AICR 1500mA Mode	$I_{AICR\_1500mA\_CHG}$	I_{AICR} = 1500mA, V_{CHG_VIN} = 5V, V_{BAT} = 3.8V	1300	1400	1500	mA
CHG_VIN UVLO	V_{UVLO_CHG}	V_{CHG_VIN} rising	3.05	3.3	3.55	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CHG_VIN UVLO Hysteresis	$V_{UVLO\_HYS\_CHG}$	V_{CHG_VIN} falling	--	150	--	mV
CHG_VIN Over-Voltage Protection Threshold	$V_{CHG\_VIN\_OVP\_CHG}$	V_{CHG_VIN} rising	13.5	14.5	15.5	V
CHG_VIN Over-Voltage Protection Hysteresis	$V_{CHG\_VIN\_OVP\_HYS\_CHG}$	V_{CHG_VIN} falling	--	250	--	mV
VBAT Over-Voltage Protection Threshold	$V_{BAT\_OVP\_CHG}$	V_{BAT} rising, as percentage of V_{OREG_CHG}, as V_{BAT_OVP}/V_{OREG_CHG}	106	108	110	%
VBAT Over-Voltage Protection Hysteresis	$V_{BAT\_OVP\_HYS\_CHG}$	V_{BAT} falling, as $(V_{BAT\_OVP\_HYS})/V_{OREG\_CHG}$	--	4	--	%
Thermal Regulation Threshold	t_{THREG_CHG}	Charge current starts decreasing (default)	--	120	--	°C
VSYS Over-Voltage Protection Threshold	$V_{SYS\_OVP\_CHG}$	V_{SYS} rising	4.9	5.25	5.5	V
VSYS Under-Voltage Protection	$V_{SYS\_UVP\_CHG}$	V_{SYS} falling	2.2	2.4	2.6	V
End of Charge						
Battery Regulation Voltage Range	V_{OREG_CHG}	I^2C programmable in 10mV steps	3.9	--	4.71	V
Battery Regulation Voltage Accuracy	$V_{OREG\_ACC\_CHG}$	V_{OREG_CHG} = 4.2V, 4.35V, 4.36V, 4.37V or V_{OREG_CHG} = 4.38V (T_C = 0°C to 70°C) (3)	-0.5	--	0.5	%
Re-charge Mode Threshold	V_{RECH_CHG}	I^2C programmable, V_{BAT} falling, the difference below V_{OREG_CHG}	50	100	150	mV
Re-charge Deglitch Time	$t_{D\_RECH\_CHG}$	V_{BAT} falling	--	120	--	ms
End-of-charge Current	I_{EOC_CHG}	I^2C programmable in 50mA steps	100	--	850	mA
Default End-of-charge Current	$I_{EOC\_DEF\_CHG}$	Default.	--	250	--	mA
End-of-charge Current Accuracy	I_{EOC_ACC}	I_{EOC_CHG} = 100 to 850mA	-20	--	20	%
End-of-charge Deglitch Time	$t_{D\_EOC\_CHG}$	I^2C default, $I_{CHG} < I_{EOC\_CHG}$, $V_{BAT} > V_{RECH\_CHG}$	--	2	--	ms
Charge Current	I_{CHG}	I^2C programmable in 0.1A steps, 0x17 bit[7:2]	0.5	--	5	A
ICHG Current Accuracy 1	$I_{CHG\_ACC1\_CHG}$	V_{BAT} = 3.8V, I_{CHG} = 500mA, (T_C = -30°C to 65°C)	-20	--	20	%
ICHG Current Accuracy 2	$I_{CHG\_ACC2\_CHG}$	V_{BAT} = 3.8V, 500mA < I_{CHG} < 1000mA, (T_C = -30°C to 65°C)	-10	--	10	%
ICHG Current Accuracy 3	$I_{CHG\_ACC3\_CHG}$	V_{BAT} = 3.8V, I_{CHG} > 1000mA, (T_C = -30°C to 65°C)	-7	--	7	%
Pre-Charge Mode Threshold	V_{PRECHG_CHG}	I^2C programmable in 0.1V steps, rising	2.0	--	3.5	V
Pre-Charge Mode Hysteresis	$V_{PRECHG\_HYS\_CHG}$	Pre-charge hysteresis, falling	--	0.2	--	V
Pre-Charge Threshold Accuracy	$V_{PRECHG\_ACC\_CHG}$	$V_{BAT} < V_{PREC\_CHG}$	-5	--	5	%
Pre-Charge Current	I_{PRECHG_CHG}	I^2C programmable (default)	--	150	--	mA
Pre-Charge Current Accuracy	$I_{PRECHG\_ACC\_CHG}$		-20	--	20	%
VSYS Regulation Voltage	$V_{SYS\_MIN\_CHG}$	I^2C programmable in 0.1V steps	3.3	--	4	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VSYS Regulation Voltage Accuracy	$V_{SYS\_MIN\_ACC\_CHG}$		-3	--	3	%
UUG On-Resistance	$R_{ON\_UUG\_CHG}$	From VBUS to CHG_VMID	--	14	30	mΩ
UG On-Resistance	$R_{ON\_UG\_CHG}$	From CHG_VMID to CHG_VLX	--	28	40	mΩ
LG On-Resistance	$R_{ON\_LG\_CHG}$	From CHG_VLX to PGND	--	28	40	mΩ
PPMOS On-Resistance	$R_{ON\_PPMOS\_CHG}$	From VSYS to VBAT	--	13	30	mΩ
Switching Frequency	f_{OSC1_CHG}	I²C programmable to 1.5 MHz	--	1.5	--	MHz
Switching Frequency Accuracy	$f_{OSC\_ACC\_CHG}$		-10	--	10	%
Maximum Duty Cycle	D_{MAX_CHG}		--	97	--	%
Minimum Duty Cycle	D_{MIN_CHG}		0	--	--	%
VDDP Regulation	V_{VDDP_CHG}	V_{BUS} = 5V	4.5	4.9	5.3	V
Buck OCP Current	$I_{BUCK\_OCP\_CHG}$	REG0x1D[2] = 1'b0	4	6	8	A
		REG0x1D[2] = 1 'b1	5.6	8	10.4	
Sink Current for Battery Detection	$I_{BAT\_SINK\_CHG}$		--	300	--	µA
Internal QONB Pull-Up Resistance	R_{QONB_CHG}		90	125	160	kΩ
QONB Exit Shipping Mode Duration	$t_{SHIPMODE\_CHG}$	CHG_QONB Low for BATFET on-time to exit shipping mode	0.81	0.9	0.99	s
QONB System Reset Duration	$t_{QONB\_RST\_CHG}$	CHG_QONB low time to enable full system reset	12	15	18	s
BATFET Reset Time	$t_{BATFET\_RST\_CHG}$	BATFET off-time during full system reset	0.54	0.6	0.66	s
Shipping Mode Entry Deglitch Time	$t_{D\_SHIP\_ENTER}$	Enter shipping mode delay	--	9	--	s
AICL	V_{AICL_CHG}	V_{BUS} rising, I²C programmable	--	4.6	--	V
AICL Hysteresis	$V_{AICL\_HYS\_CHG}$		--	50	--	mV
OTG Output Regulation	V_{BSTCV_CHG}	I²C programmable default	--	5.05	--	V
OTG Output Accuracy	$V_{BSTCV\_ACC\_CHG}$	I_{VBUS} = no load, VOBST = 5.05V	-3	--	3	%
OTG Over-Load Protection Threshold	$I_{BST\_0.5A\_CHG}$	REG0x1A[2:0] = 3'b000	0.5	0.55	0.6	A
OTG CHG_VMID Over-Voltage Protection Threshold	$V_{MIDOVP\_OTG\_CHG}$	V_{CHG_VMID} rising	4.2	6	--	V
OTG CHG_VMID Over-Voltage Protection Hysteresis	$V_{MIDOVP\_OTG\_HYS\_CHG}$		--	200	--	mV
OTG VBAT Under-Voltage Protection Threshold	$V_{BAT\_UVP\_OTG\_CHG}$	I²C default, VBAT falling	--	2.8	3.08	V
OTG VBAT Under-Voltage Protection Hysteresis	$V_{BAT\_UVP\_OTG\_HYS\_CHG}$	Rising	--	400	--	mV
OTG Over-Current Protection Threshold	$I_{OTG\_OCP\_CHG}$	Default = 6.05A	5.2	6.05	6.9	A
Battery Temperature HOT Threshold	$V_{VTS\_HOT\_CHG}$	V_{TS} falling, the ratio of CHG_VDDP	33.5	34.5	35.5	%VTS
Battery Temperature WARM Threshold	$V_{VTS\_WARM\_CHG}$	V_{TS} falling, the ratio of CHG_VDDP	44	45	46	%VTS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Battery Temperature COOL Threshold	$V_{VTS\_COOL\_CHG}$	V_{TS} rising, the ratio of CHG_VDDP	67.5	68.5	69.5	%VTS
Battery Temperature COLD Threshold	$V_{VTS\_COLD\_CHG}$	V_{TS} rising, the ratio of CHG_VDDP	72.5	73.5	74.5	%VTS
Battery Temperature Hysteresis	$V_{VTS\_HYS\_CHG}$		--	2	--	%VTS
VDP_SRC Voltage	$V_{DP\_SRC\_CHG}$	With IDAT_SRC = 0 to 250µA	0.5	--	0.7	V
VDAT_REF Voltage	$V_{DAT\_REF\_CHG}$		0.25	--	0.4	V
VLGC Voltage	V_{LGC_CHG}		0.8	--	2	V
IDM SINK Current	IDM_SINK	May be a resistance if desired	50	100	150	µA
Data Contact Timeout	t_{DCDT}	Setting by register 0x22[5:4]	--	600	--	ms
Dedicated Charging Port resistance across D+/-	$R_{D+D-\ DCP}$	REG0x24[1] = 1'b1	50	90	130	Ω
Pull-Down Resistance on CHG_OTG	$R_{L\_CHG\_OTG}$		--	100	--	kΩ
Pull-Down Resistance on CHG_ENB	R_{CHG_ENB}		--	100	--	kΩ
ADC						
ADC Conversion Time	t_{CONV_ADC}	One channel	35	--	200	ms
Number of Bits for ADC Resolution	R_{ES_ADC}		--	10	--	bits
VBUS_DIV5 Measurement Range	$V_{VBUS\_DIV5\_ADC\_RANGE}$		1	--	22	V
VBUS_DIV5 Resolution	$V_{VBUS\_DIV5ADC\_RES}$		--	25	--	mV
VBUS_DIV5 Accuracy	$V_{VBUS\_DIV5ADC\_ACC}$		-3	--	3	LSB
VBUS_DIV2 Measurement Range	$V_{VBUS\_DIV2\_ADC\_RANGE}$		1	--	9.7	V
VBUS_DIV2 Resolution	$V_{VBUS\_DIV2ADC\_RES}$		--	10	--	mV
VBUS_DIV2 Accuracy	$V_{VBUS\_DIV2ADC\_ACC}$		-3	--	3	LSB
VBAT Measurement Range	$V_{BAT\_ADC\_RANGE}$		0	--	4.9	V
VBAT Resolution	$V_{BAT\_ADC\_RES}$		--	5	--	mV
VBAT Accuracy	$V_{BAT\_ADC\_ACC}$		-2	--	2	LSB
VSYS Measurement Range	$V_{SYS\_ADC\_RANGE}$		0	--	4.9	V
VSYS Resolution	$V_{SYS\_ADC\_RES}$		--	5	--	mV
VSYS Accuracy	$V_{SYS\_ADC\_ACC}$		-2	--	2	LSB
CHG_VDDP Measurement Range	$V_{CHG\_VDDP\_ADC\_RANGE}$		0	--	4.9	V
CHG_VDDP Resolution	$V_{CHG\_VDDP\_ADC\_RES}$		--	5	--	mV
CHG_VDDP Accuracy	$V_{CHG\_VDDP\_ADC\_ACC}$		-2	--	2	LSB
TS_BAT Measurement Range	$R_{ATETS\_BAT\_RANGE}$		0	--	100	%
TS_BAT Resolution	$R_{ATETS\_BAT\_RES}$		--	0.25	--	%
TS_BAT Accuracy	$R_{ATETS\_BAT\_ACC}$		-2	--	2	LSB
IBUS Measurement Range	$I_{IBUS\_ADC\_RANGE}$		0	--	5	A
IBUS Resolution	$I_{IBUS\_ADC\_RES}$		--	50	--	mA
IBUS Accuracy	$I_{IBUS\_ADC\_ACC}$	I_{BUS} > 2A, IAICR [5:0] setting ≥ 400mA	-3	--	3	LSB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
		I_{BUS} < 2A, IAICR [5:0] setting ≥ 400mA	-2	--	2	
		I_{BUS} < 2A, IAICR [5:0] setting < 400mA	-2	--	2	
IBAT Measurement Range	$I_{IBAT\_ADC\_RANGE}$		0	--	5	A
IBAT Resolution	$I_{IBAT\_ADC\_RES}$		--	50	--	mA
IBAT Accuracy	$I_{IBAT\_ADC\_ACC}$		-2	--	2	LSB
TEMP_JC Measurement Range	$T_{TEMP\_JC\_ADC\_RANGE}$		-40	--	120	°C
TEMP_JC Resolution	$T_{TEMP\_JC\_ADC\_RES}$		--	2	--	°C
TEMP_JC Accuracy	$T_{TEMP\_JC\_ADC\_ACC}$	Temperature < 85°C	-2	--	2	LSB
Pump Express						
PE+1 On Time (A)	$t_{ON\_A\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	430	500	570	ms
PE+1 On Time (B)	$t_{ON\_B\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	240	300	360	ms
PE+1 On Time (C)	$t_{ON\_C\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	70	100	130	ms
PE+1 Off Time (D)	$t_{OFF\_D\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	70	100	130	ms
PE+1 Off Time (I)	$t_{OFF\_I\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	80	--	225	ms
PE+2 Off Time (D)	$t_{OFF\_D\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	87	105	128	ms
PE+2 On Time (E)	$t_{ON\_E\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	147	190	248	ms
PE+2 On Time (F)	$t_{ON\_F\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	87	102.5	118	ms
PE+2 On Time (G)	$t_{ON\_G\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	22	50	68	ms
PE+2 Off Time (H)	$t_{OFF\_H\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	22	50	68	ms
PE+2 Off Time (I)	$t_{OFF\_I\_PE}$	V_{BAT} = 3.8V. Use PE+ adapter	135	155	175	ms
Flash LED Current Source						
LED Current Accuracy	$I_{LED1\_ACC\_FL}$	Flash LED current is set 25mA to 400mA	-8	--	8	%
LED Current Accuracy	$I_{LED2\_ACC\_FL}$	Flash LED current set 0.4A to 1A	-6	--	6	%
FL_LEDCSx Leakage Current	I_{LEAK_FL}	VLEDVIN = 5V, LEDCSX = 0, LEDCSX disabled	--	0.1	4	µA
FL_LEDCSx Start Up Current	I_{START_FL}	LEDCSX = 0, LEDCSX enabled	--	320	1000	µA
LEDCSX Short Threshold	V_{SC_FL}		--	1	1.3	V
LEDCSX Short Event Timer	$t_{D\_SC\_FL}$		1.8	2.5	3.3	ms
Flash Time-Out	$t_{TIMEOUT\_FL}$	FLEDx_STRB_TO = 0100101	--	1248	--	ms
Flash Timer Accuracy	$t_{TMR\_ACC\_FL}$	Timer set by register	-10	--	10	%
Current Source Regulation Voltage	V_{REG1_FL}	I_{LED} = 200mA, 0x7C[1:0] = 00	--	200	300	mV
Current Source Regulation Voltage	V_{REG2_FL}	I_{LED} = 1500mA, 0x7C[1:0] = 01	--	--	500	mV
Strobe/TXMask Deglitch Time	$t_{D\_STRB\_FL}$		--	10	--	µs
Flash Ready Time	$t_{FLSH\_RDY\_FL}$	EN_LEDCS = 1 to current reach 800mA target value	--	4.5	5	ms
Strobe FL-CHG_VIN OVP	VIN_OVP_FL		5.45	5.6	5.75	V
Strobe FL-CHG_VIN OVP Hysteresis	VIN_OVP_Hys_FL		0.25	0.3	0.35	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Timer Accuracy	$t_{D\_ACC\_FL}$	V_{DDA} = 2.7V to 5.5V (for deglitch time, soft-start)	--	10	15	%
High Side Switch On-Resistance	$R_{ON\_H\_FL}$		--	60	--	mΩ
Low Side Switch On-Resistance	$R_{ON\_L\_FL}$		--	36	--	mΩ
Pull-Down Resistance on FL_STROBE	$R_{L\_FL\_STROBE}$		--	350	--	kΩ
Pull-Down Resistance on BL_EN	$R_{L\_FL\_TORCH}$		--	350	--	kΩ
Pull-Down Resistance on FL_TXMASK	$R_{L\_FL\_TXMASK}$		--	300	--	kΩ
Backlight						
Maximum Backlight LED Current	$I_{LED\_MAX\_BL}$	Maximum LED current (per string)	--	30	--	mA
Backlight LED Current Accuracy	$I_{LED\_ACC\_BL}$	2.7V ≤ V_{SYS} ≤ 5V, 6mA < I_{LED} < 30mA, Linear or Exponential Mode	-3	--	3	%
		2.7V ≤ V_{SYS} ≤ 5V, 0.1mA < I_{LED} < 6mA, Linear or Exponential Mode	-10	--	10	%
Backlight LED Current Matching	$I_{LED\_MATCH\_BL}$	2.7V ≤ V_{SYS} ≤ 5V, 100µA < I_{LED} < 30mA, Linear or Exponential Mode	-3	0.2	3	%
Minimum Backlight LED Current	$I_{LED\_MIN\_LINEAR\_BL}$	PWM or I^2C current control linear mode (per string) (3)	--	14.6	--	µA
Minimum Backlight LED Current	$I_{LED\_MIN\_EXP\_BL}$	PWM or I^2C current control exponential mode (3)	--	60	--	µA
LED Current Step size	$I_{LED\_STEP\_EXP\_BL}$	Exponential mode (Code to Code)	--	0.3	--	%
LED Current Step size	$I_{LED\_STEP\_LINEAR\_BL}$	Linear mode (Code to Code)	--	14.6	--	µA
Backlight Output Over-Voltage Protection Threshold	V_{OVP_BL}	2.7V ≤ VCHG_VIN ≤ 5V, rising. BLED_OVP @ REG0xA1[6:5] = 2'b01	19.8	21	22.2	V
Regulated Current Sink Headroom Voltage (Boost Feedback Voltage)	V_{HR_BL}	I_{LED} = 3 mA	--	500	--	mV
N-MOSFET On-Resistance	$R_{ON\_N\_BL}$	I_{SW} = 500mA	--	0.2	--	Ω
Switching Frequency	f_{SW_BL}	2.7V ≤ V_{IN} ≤ 5V	450	500	550	kHz
		2.7V ≤ V_{IN} ≤ 5V	900	1000	1100	kHz
N-MOSFET Current Limit Tolerance	$I_{LIM\_NMOS\_BL}$	2.7V ≤ V_{IN} ≤ 5V @ REG0xA1[2:1] : BL_OC = 2'b01	960	1200	1440	mA
Maximum Boost Duty Cycle	$D_{MAX\_BST\_BL}$		92	96	--	%
PWM Input Frequency Range	f_{PWM_BL}	2.7V ≤ V_{IN} ≤ 5V	50	--	50000	Hz
Minimum Pulse ON Time	$t_{ON\_MIN\_BL}$	Sample rate = 24MHz	183.3	--	--	ns
		Sample rate = 4MHz	1100	--	--	
		Sample rate = 1MHz	5500	-	--	
Minimum Pulse OFF Time	$t_{OFF\_MIN\_BL}$	Sample rate = 24MHz	183.3	--	--	ns
		Sample rate = 4MHz	1100	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
		Sample rate = 1MHz	5500	--	--	
Turn on Delay from PWM = 0 to PWM = 50% Duty Cycle	$t_{START\_UP\_BL}$	24MHz sample rate, FPWM = 10kHz	--	6	9	ms
PWM Shutdown Period	$t_{PWM\_STBY\_BL}$	Sample rate = 24MHz	0.54	0.60	0.66	ms
		Sample rate = 4MHz	0.27	3	3.3	
		Sample rate = 1MHz	22.5	25	27.5	
Pull-Down Resistance on PWM	R_{L_BLPWM}	Pull-down resistance on PWM	--	335	--	kΩ
Pull-Down Resistance on BL_EN	R_{L_BLEN}		--	388	--	kΩ
PWM Input Resolution	R_{ESPWM_BL}	50Hz < FPWM < 11kHz	--	--	11	bits
Display Bias						
Positive Voltage Accuracy	$V_{POSV\_ACC\_DB}$	REG0XB3[5:0] = 6'b011100, I_{OUT} = 0mA	-1	--	1	%
Negative Voltage Accuracy	$V_{NEGV\_ACC\_DB}$	REG0XB4[5:0] = 6'b011100, I_{OUT} = 0mA	-1.5	--	1.5	%
POS Ripple	V_{RIPPLE_POS}	REG0xB2[5:0] = 0'b100010, REG0XB3[5:0] = 0'b011110, I_{OUT} = 0mA	--	20	--	mV
NEG Ripple	V_{RIPPLE_NEG}	REG0xB2[5:0] = 0'b100010, REG0xB4[5:0] = 0'b011110, I_{OUT} = 0mA	--	75	--	mV
Display Bias LDO Dropout Voltage	V_{DROP_DB}	V_{DB_BST} = V_{DB_POS} = 5.2V, I_{OUT} = 80mA	--	35	70	mV
BST Switching Frequency	f_{SW_DB}		0.9	1.0	1.1	MHz
Maximum Duty Cycle	D_{MAX_DB}		90	91	--	%
BST N-MOSFET On-Resistance	$R_{ON\_N\_DB}$		0.05	0.3	0.6	Ω
BST P-MOSFET On-Resistance	$R_{ON\_P\_DB}$	REG0XB2[5:0] = 6'b100010	0.05	0.5	1	Ω
Charge Pump Equivalent Resistance	$R_{EQ\_CP\_DB}$	$V_{DB\_BSTVOUT}$ = 5.2V, I_{NEG} = 50mA	--	2.4	--	Ω
POS Discharge Resistor	R_{DISCHP_DB}	REG0xB1[5] = 1'b1	--	70	--	Ω
NEG Discharge Resistor	R_{DISCHN_DB}	REG0xB1[2] = 1'b1	--	20	--	Ω
BST Current Limit	I_{BSTOCP_DB}	REG0xB2[5:0] = 6'b100010	0.88	1.1	1.32	A
POS Short-Circuit Protection Voltage	V_{SCPP_DB}		--	0.8 x DB_VPOS	--	V
NEG Short-Circuit Protection Voltage	V_{SCPN_DB}		--	0.25 - 0.8 x DB_VNEG	--	V
Pull-Down Resistance on DB_ENN	$R_{L\_DB\_ENN}$		--	386	--	kΩ
Pull-Down Resistance on DB_ENP	$R_{L\_DB\_ENP}$		--	386	--	kΩ
USB_PD						
Bit Rate	$f_{BitRate\_PD}$		270	300	330	Kbps
Maximum difference between the bit rate during the part of the packet following the Preamble and the reference bit-rate.	$p_{BitRate\_PD}$		--	--	0.25	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Time from the end of last bit of a frame until the start of the first bit of the next Preamble.	$t_{InterFrameGap\_PD}$		25	--	--	µs
Time before the start of the first bit of the Preamble when the transmitter shall start driving the line	$t_{StartDrive\_PD}$		-1	--	1	µs
Time to cease driving the line after the end of the last bit of the frame.	$t_{EndDriveBMC\_PD}$		--	--	23	µs
Fall Time	t_{Fall_PD}		300	--	--	ns
Time to cease driving the line after the final high-to-low transition	$t_{HoldLowBMC\_PD}$		1	--	--	µs
Rise Time	t_{Rise_PD}		300	--	--	ns
Voltage Swing	V_{Swing_PD}		1.05	1.125	1.2	V
Transmitter Output Impedance	z_{Driver_PD}		33	--	75	Ω
Time window for detecting non-idle	$t_{TransitionWindow\_PD}$		12	--	20	µs
Receiver Input Impedance	z_{BmcRx_PD}		1	--	--	MΩ
Operating Supply Current	I_{OP_PD}	Cable attached (Full function on)	--	2.8	--	mA
Idle Mode Current (Act as a source)	$I_{IDLE\_SRC1\_PD}$	Cable attached with Ra, Rd	--	300	--	µA
Idle Mode Current (Act as a source)	$I_{IDLE\_SRC2\_PD}$	Cable attached with either Ra or Rd	--	200	--	µA
Idle Mode Current (Act as a sink)	$I_{IDLE\_SNK\_PD}$	Cable attached	--	125	--	µA
Low-Power Mode	$I_{LOW-POWER\_PD}$	Cable unattached, $V_{PD\_VCONN5V}$ = 5V	--	20	--	µA
		Cable unattached, $V_{PD\_VCONN5V}$ = 0V	--	10	--	
Shipping-Mode Current	I_{SHIP_PD}		--	1	--	µA
VCONN Switch On-Resistance	$R_{ON\_VCONN\_PD}$		--	0.7	1	Ω
OCP Range	I_{OCP_PD}		200	--	600	mA
Time for VCONN Switch to Turn-On State	$t_{D\_SOFT\_PD}$		--	1.2	--	ms
DFP 80µA CC Current	$I_{CC\_DFP80µ\_PD}$		64	80	96	µA
DFP 180µA CC Current	$I_{CC\_DFP180µ\_PD}$		166	180	194	µA
DFP 330µA CC Current	$I_{CC\_DFP330µ\_PD}$		304	330	356	µA
UFP Pull-Down Resistance through CC Pin	Rd_{PD}		4.59	5.1	5.61	kΩ
UFP Pull-Down Threshold Voltage in Dead Battery	$V_{TH\_DBL\_PD}$	Under I_{CHG} = $I_{CC\_DFP80µ\_PD}$ and $I_{CC\_DFP180µ\_PD}$	0.2	--	1.6	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
UFP Pull-Down Threshold Voltage in Dead Battery	$V_{TH\_DBH\_PD}$	Under $I_{CHG} = I_{CC\_DFP330\mu\_PD}$	0.8	--	2.45	V
Valid VBUS Detection Threshold	$V_{VALID\_VBUS\_PD}$		3.5	--	4.0	V
VBUS Measurement Range	V_{VBUSMR_PD}		4	--	20	V
VBUS Measurement Step	$V_{VBUS\_MSL\_PD}$	If V_{BUS} measurement range is from 4V to 10V	--	0.5	--	V
VBUS Measurement Step	$V_{VBUS\_MSH\_PD}$	If V_{BUS} measurement range is from 10V to 20V	--	1	--	V
RGB LED Driver						
Current Accuracy	$I_{LED\_ACC\_RGB}$	I_{LED} = 4mA to 24mA	-4	--	4	%
Current Matching	$I_{LED\_MATCH\_RGB}$	I_{LED} = 4mA to 24mA	-3	--	3	%
Dropout Voltage	V_{DROP_RGB}	I_{LED} = 20mA	--	200	300	mV
LED Open-Circuit Protection Threshold	$V_{TH\_OPP\_RGB}$	Any ISINK voltage lower than open LED protection threshold	40	100	160	mV
LED Short-Circuit Protection Threshold	$V_{TH\_SCP\_RGB}$	Any ISINK voltage higher than short LED protection threshold	VSYS - 0.88	VSYS - 0.5	VSYS - 0.12	V
LDO						
Input Voltage Range	V_{IN_LDO}		2.7	--	5	V
Output Voltage Range	V_{OUT_LDO}		1.6	--	4	V
Output Voltage Accuracy	ΔV_{OUT_LDO}	$V_{IN\_LDO} = (V_{OUT\_LDO} + V_{DROP})$ to 5V, I_{OUT} = 0mA to 400mA	-3	--	3	%/V
Load Current	I_{LOAD_LDO}	$V_{IN\_LDO} = (V_{OUT\_LDO} + V_{DROP})$ to 5V	0	--	400	mA
Output Current Limit	I_{LIM_LDO}	$V_{IN\_LDO} = (V_{OUT\_LDO} + V_{DROP})$ to 5V, V_{OUT} = 70% of V_{OUT} (Target)	600	--	--	mA
Dropout Voltage	V_{DROP_LDO}	V_{IN_LDO} > 2V, I_{OUT} = 0.3A	--	--	180	mV
Load Regulation	ΔI_{LOAD_LDO}	$V_{IN\_LDO} = (V_{OUT\_LDO} + V_{DROP})$ to 5V, I_{OUT} = 1mA to 400mA	-0.2	0.06	0.2	%/mA
Line Regulation	ΔV_{LINE_LDO}	$V_{IN\_LDO} = (V_{OUT\_LDO} + V_{DROP})$ to 5V, I_{OUT} = 1mA to 400mA	-1	0.5	1	%/V
Power Supply Rejection Ratio	$PSRR_{LDO}$	V_{IN_LDO} = 3.6V, V_{OUT_LDO} = 2.8V, IOUT = 20mA @ 1kHz, LDO_COUT = 2.2µF (3)	--	50	--	dB
Inrush Current	I_{INRUSH_LDO}	I_{OUT} = 0mA, LDO_COUT = 2.2µF (3)	--	--	500	mA
Soft-Start Time	t_{SS_LDO}	I^2C Enable to V_{OUT_LDO} = 90% of V_{OUT_LDO} (Target), LDO_COUT = 2.2µF @ Forced turn-on BASE (REG0x10[1] = 1'b1) (3)	--	--	300	µs
Discharge Time	t_{DISCHG_LDO}	I^2C Disable to V_{OUT_LDO} = 10% of V_{OUT_LDO} (Target), LDO_COUT = 2.2µF (3)	--	--	500	µs
I^2C Characteristics						
LOW-Level Input Voltage	$V_{IL\_I^2C}$		--	--	0.4	V
HIGH-Level Input Voltage	$V_{IH\_I^2C}$		1.2	--	--	V
LOW-Level Output Voltage	$V_{OL\_I^2C}$	Open-drain	--	--	0.4	V
Input Current Each IO Pin	$I_{IN\_I^2C}$	0.1 x V_{DD} < V_I < 0.9 x $V_{DD(MAX)}$	-10	--	10	µA
SCL Clock Frequency	$f_{SCL\_I^2C\_HSM}$	CB ≦ 100pF	--	--	3.4	MHz
		100pF ≦ CB ≦ 400pF	--	--	1.7	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Data Hold Time	$t_{DH\_I^2C}$		30	--	--	ns
Data Set-Up Time	$t_{DS\_I^2C}$		70	--	--	ns

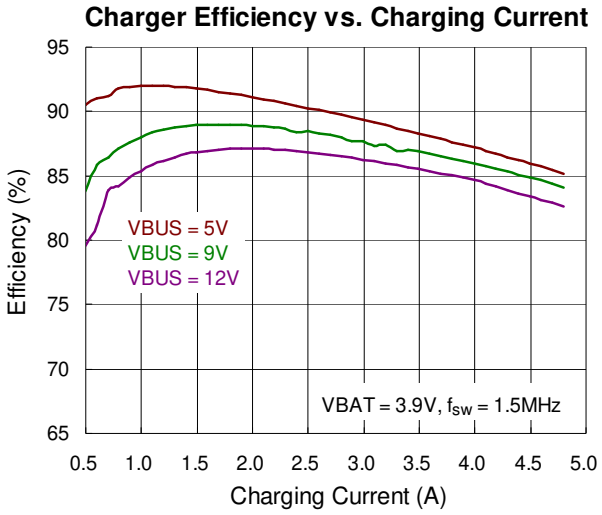
(1) Note 1 A 10kΩ NTC thermistor with β = 3435K is suggested, and a SEMITEC 103KT1608T is in use.

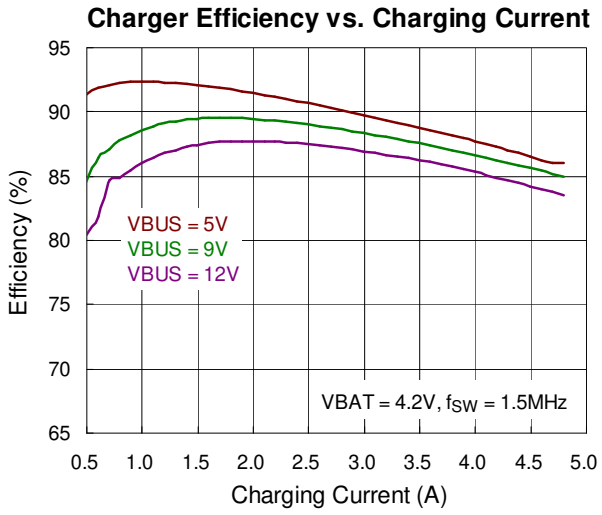
(2) Note 2 Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

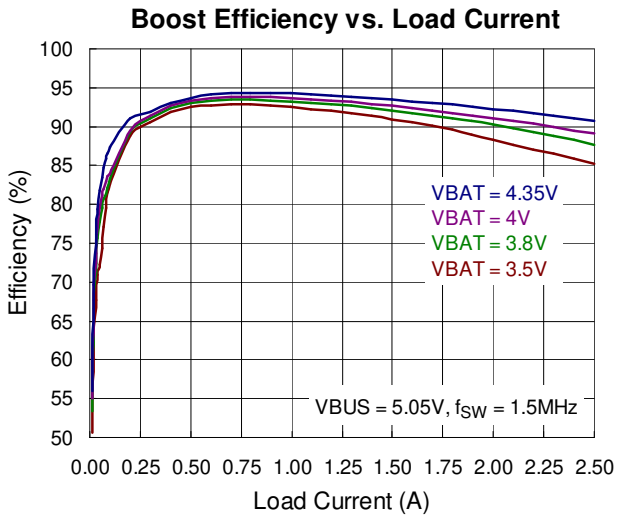
(3) Note 3 Guarantee by design.

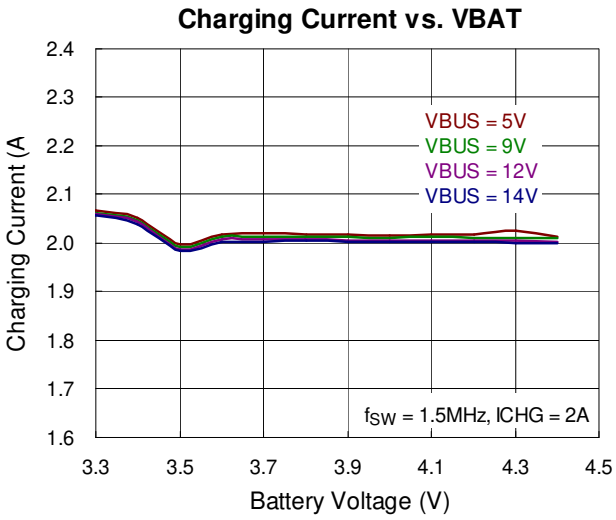
3 Typical Operating Characteristics

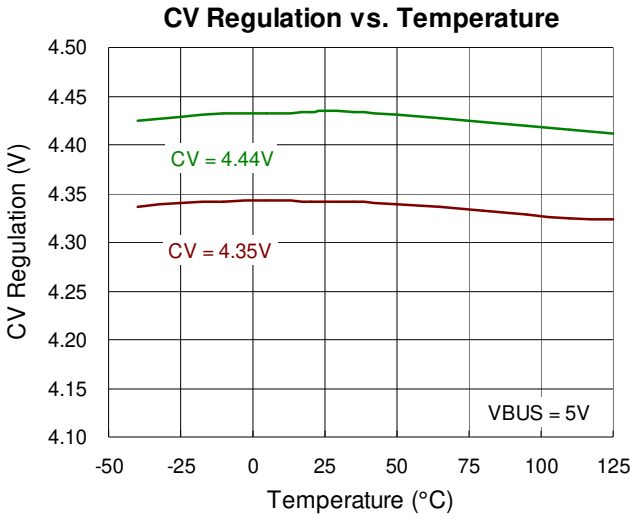
3.1 Typical Operating Characteristics

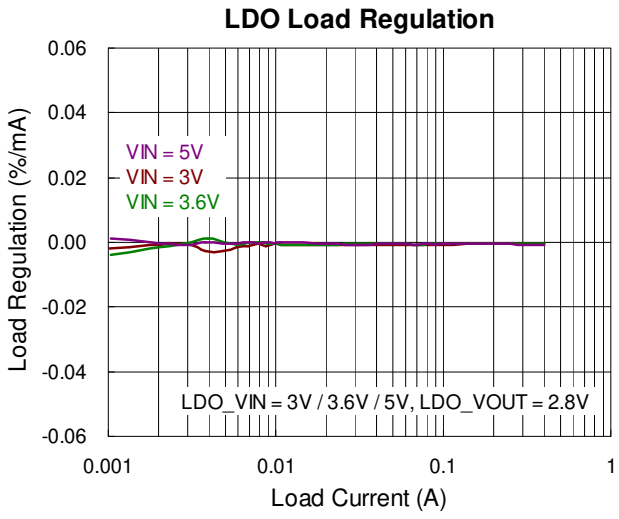


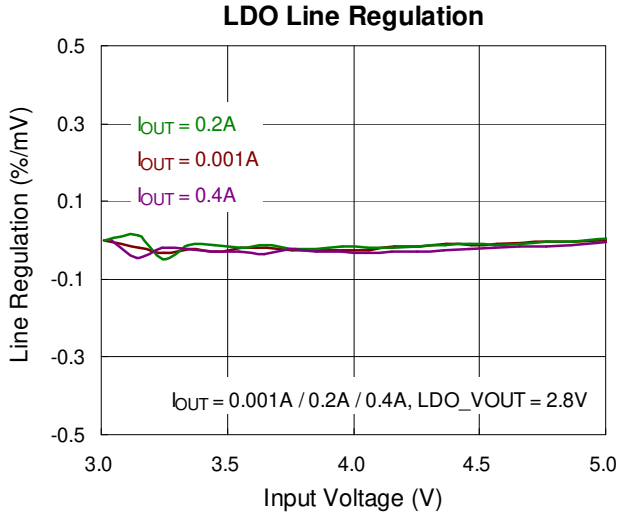


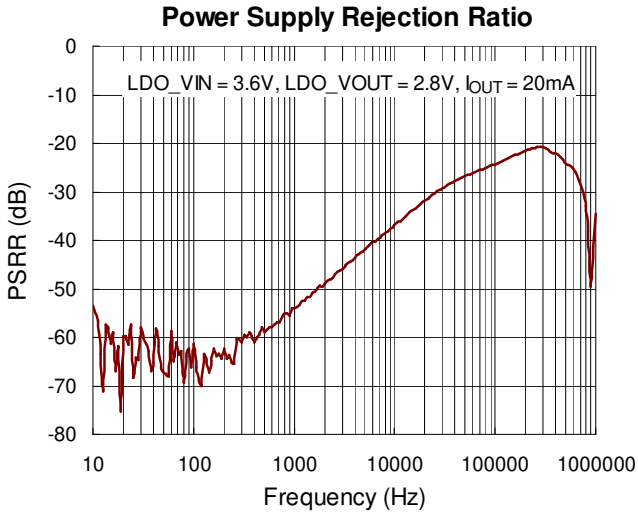


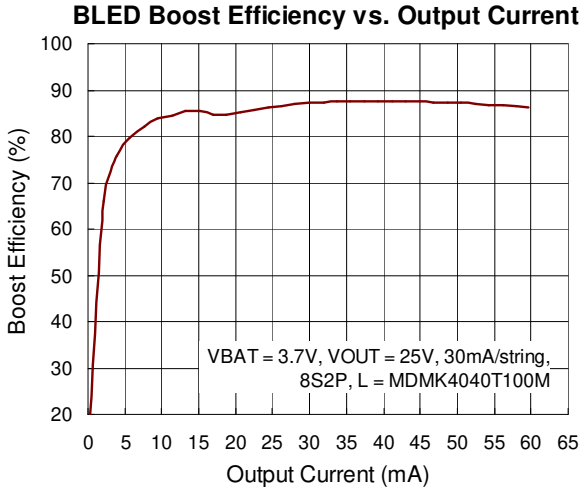


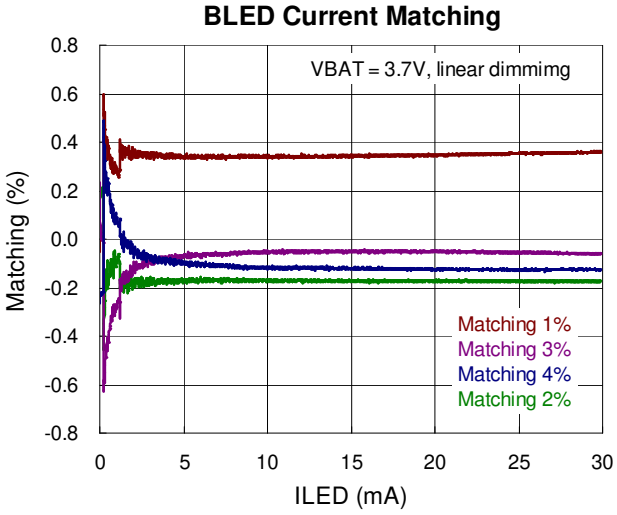


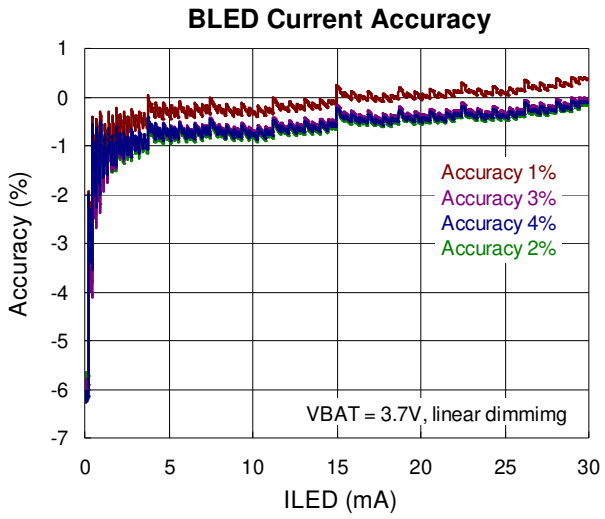


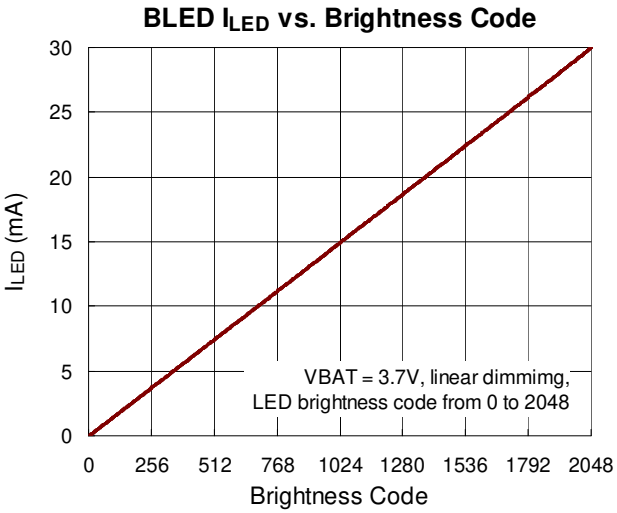


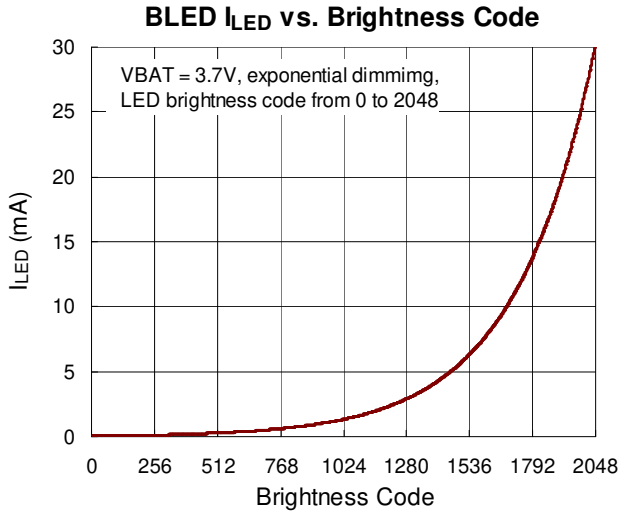


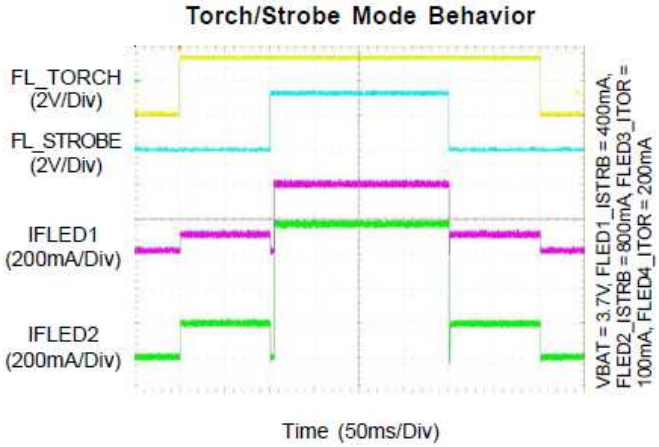


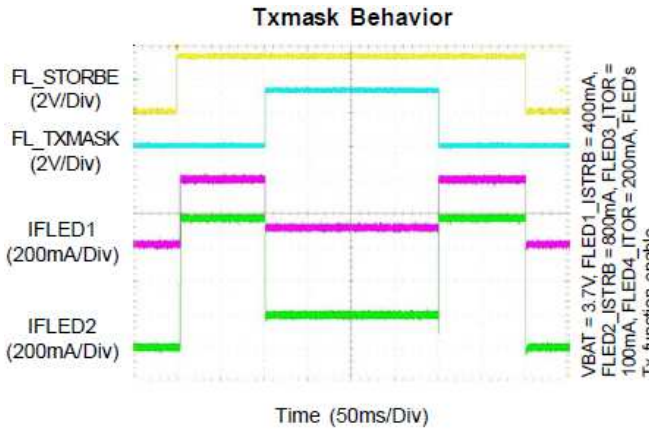


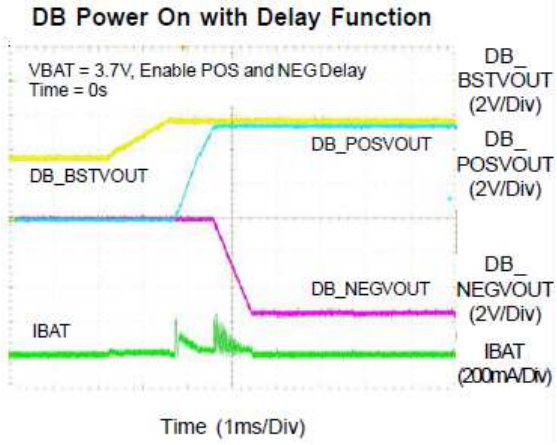












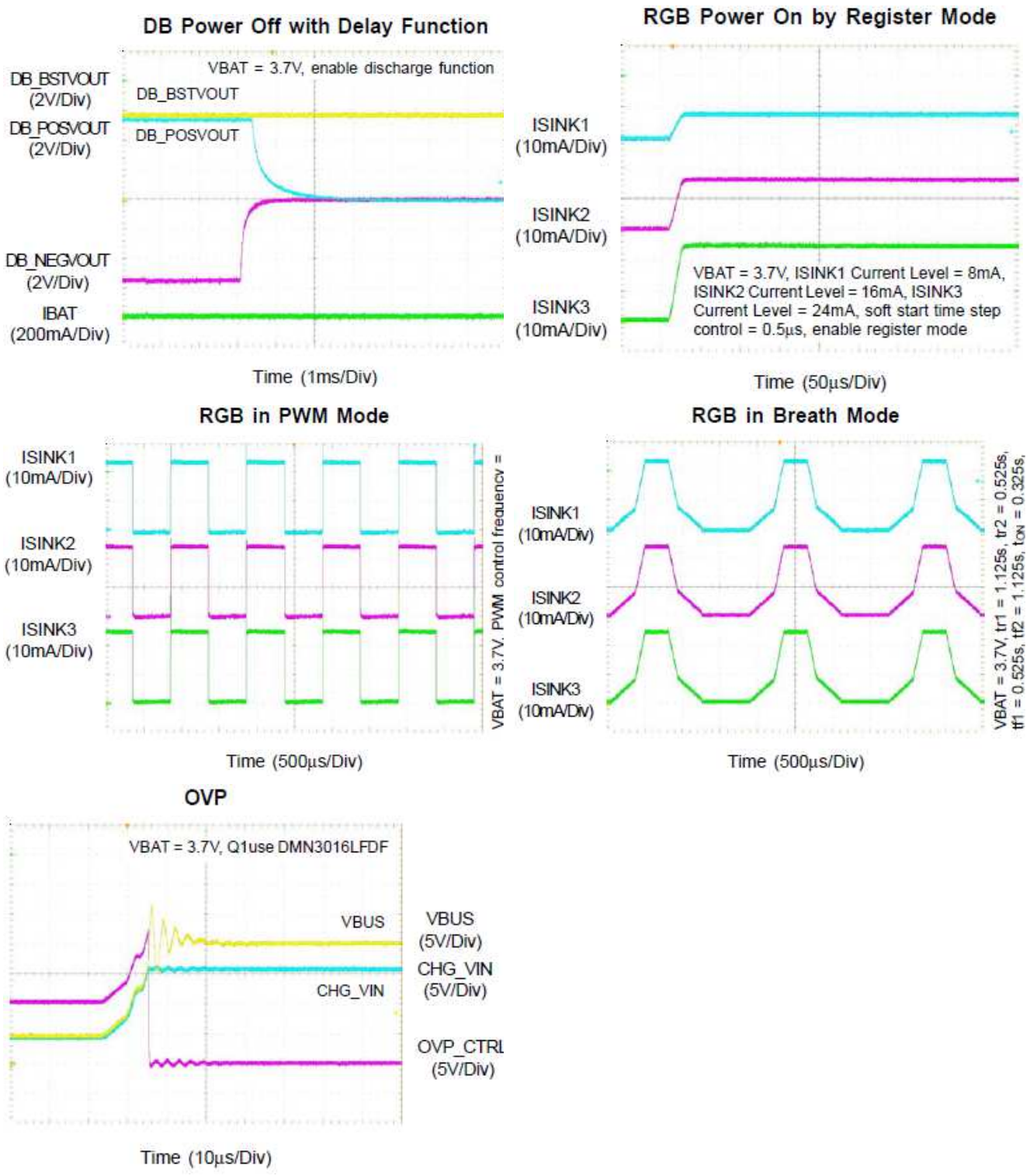
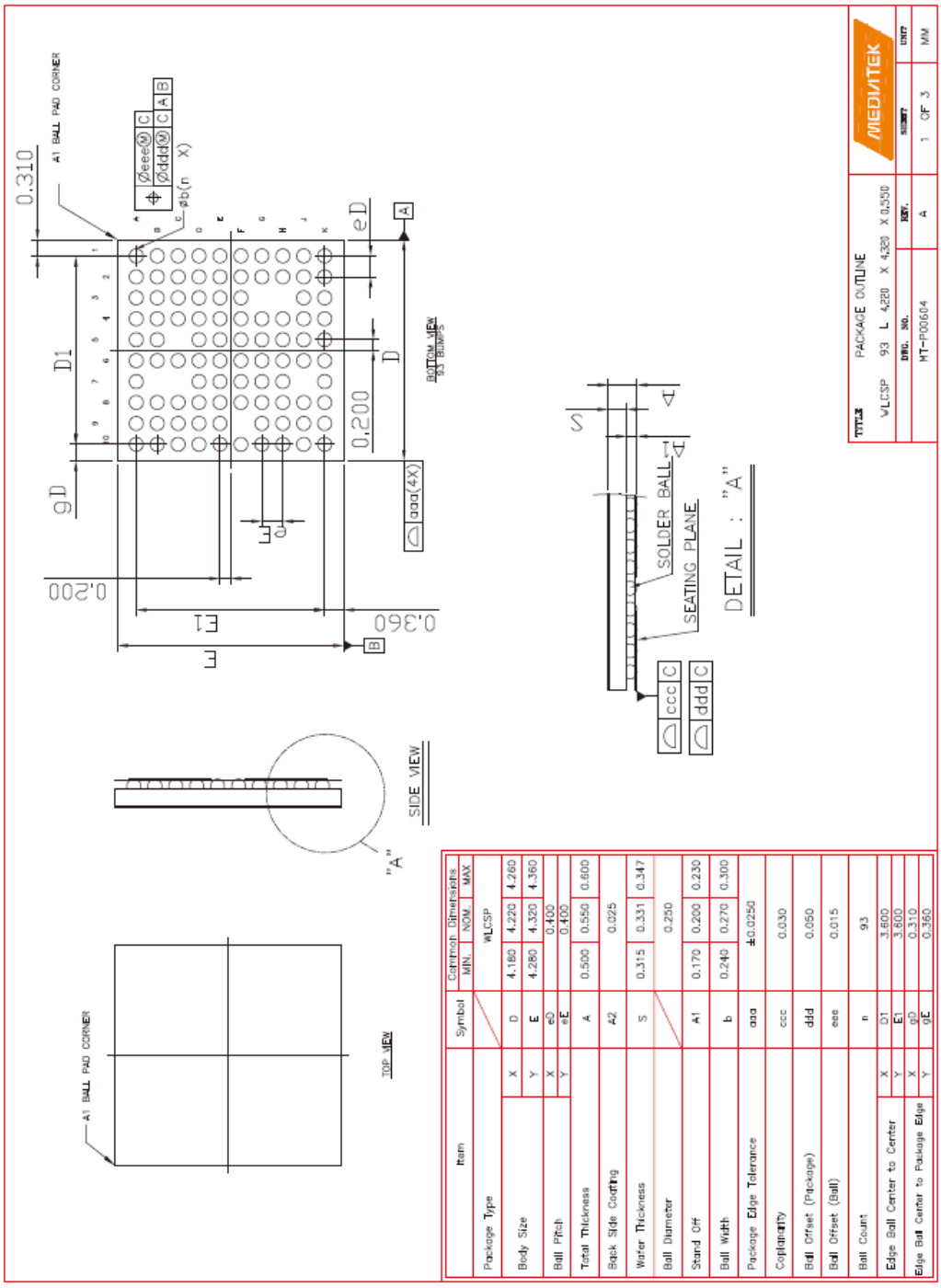


Figure 3-1. Typical operating characteristics

4 MT6370 Packaging

4.1 Outline Dimensions



Item		Symbol	Common Dimensions MIN.	NOM.	MAX
Package Type				WLCSP	
Body Size	X	D	4.180	4.220	4.260
	Y	E	4.280	4.320	4.360
Ball Pitch	X	eD		0.400	
	Y	eE		0.400	
Total Thickness		A	0.500	0.550	0.600
Back Side Coating		A2		0.025	
Wafer Thickness		S	0.315	0.331	0.347
Ball Diameter				0.250	
Stand Off		A1	0.170	0.200	0.230
Ball Width		b	0.240	0.270	0.300
Package Edge Tolerance		aaa		±0.0250	
Coplanarity		ccc		0.030	
Ball Offset (Package)		ddd		0.050	
Ball Offset (Ball)		eee		0.015	
Ball Count		n		93	
Edge Ball Center to Center	X	D1		3.600	
	Y	E1		3.600	
Edge Ball Center to Package Edge	X	eD		0.310	
	Y	gE		0.360	

Figure 4-1. Package dimension

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